

Genesys ZU

Variant: 3EG

11/13/2019

Rev B.1

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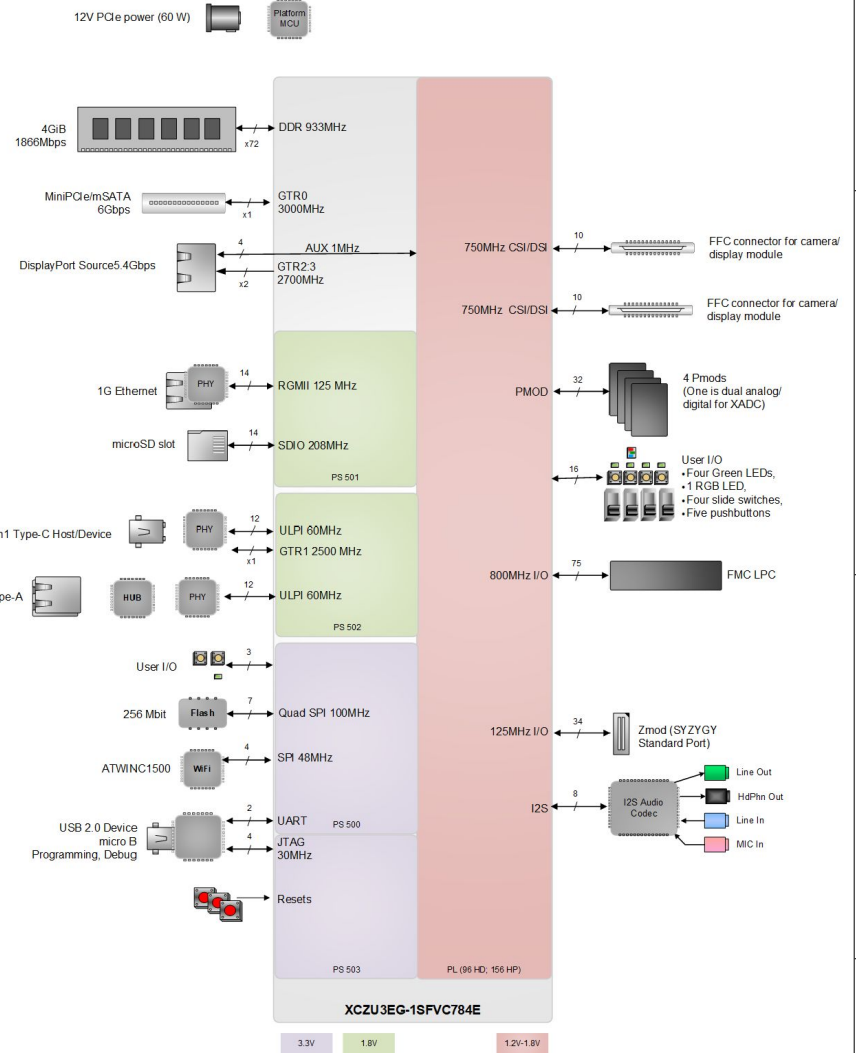
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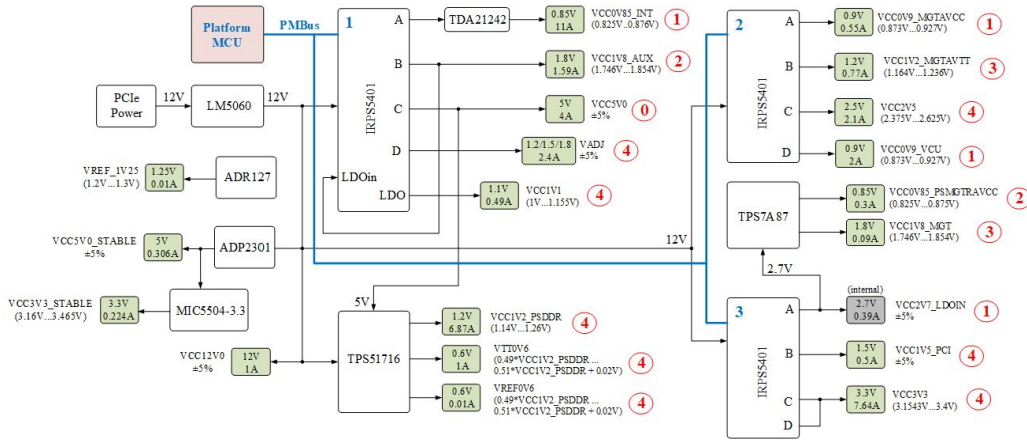
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Block Diagram



Power Tree



SHIELD F Foot F1

SHIELD F Foot F2

SHIELD F Foot F3

Foot F4

SHIELD F Foot F5

SHIELD F Foot F6

SHIELD F Foot F7

No Load F9

Foot F8

No Load F10

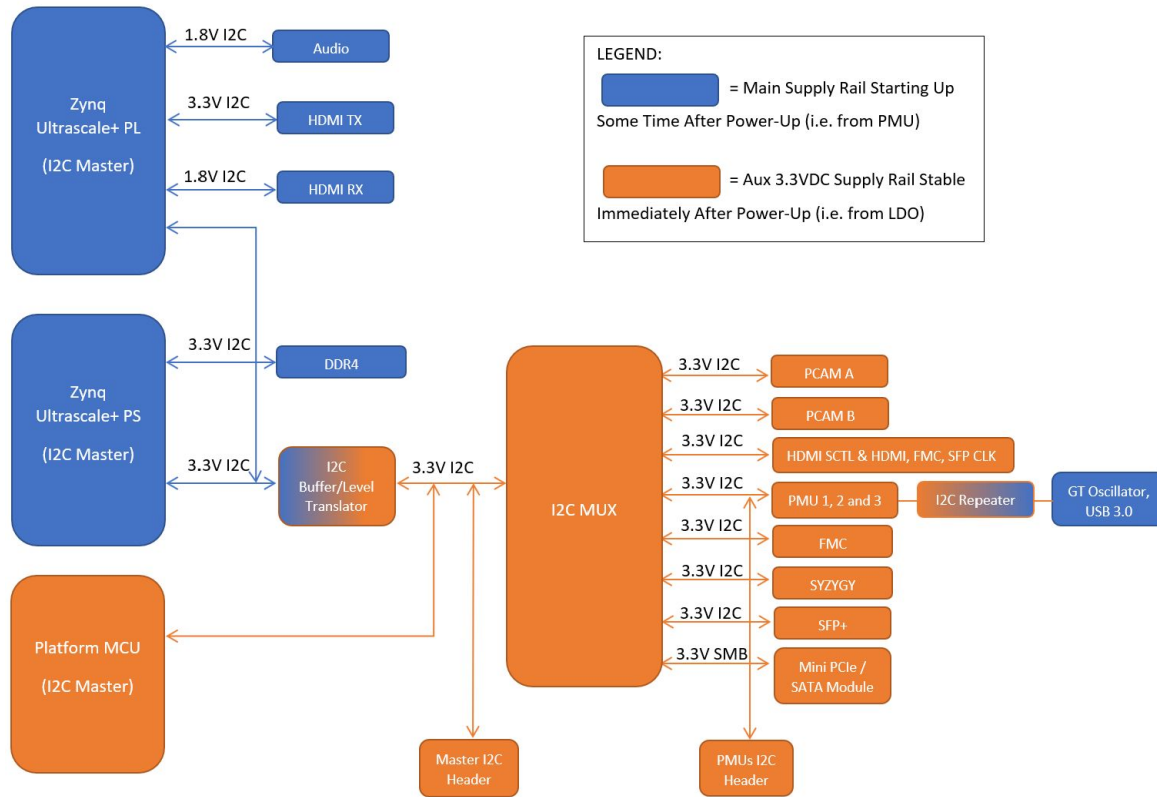
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Circuit	Block Diagram	Copyright	2019
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Genesys ZU Insert Contacts Down

Chinese ROHS ROHS Diligent Inc. CE Xilinx

I2C Diagram



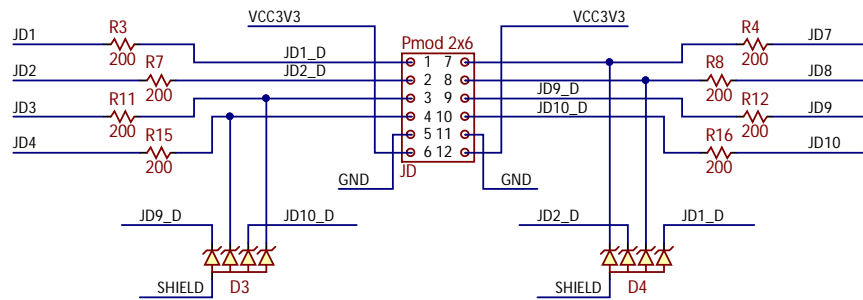
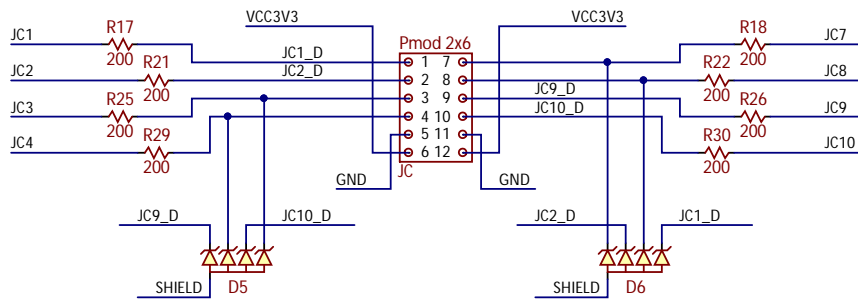
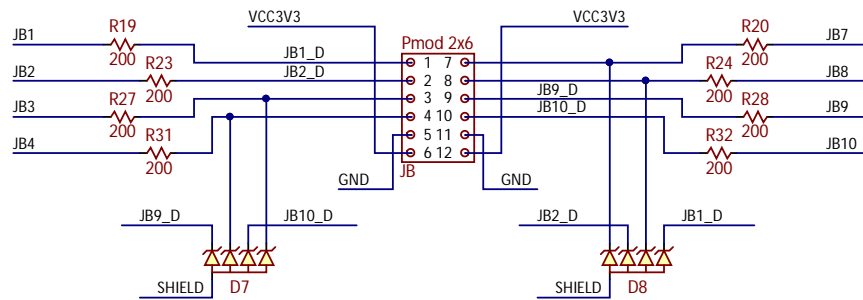
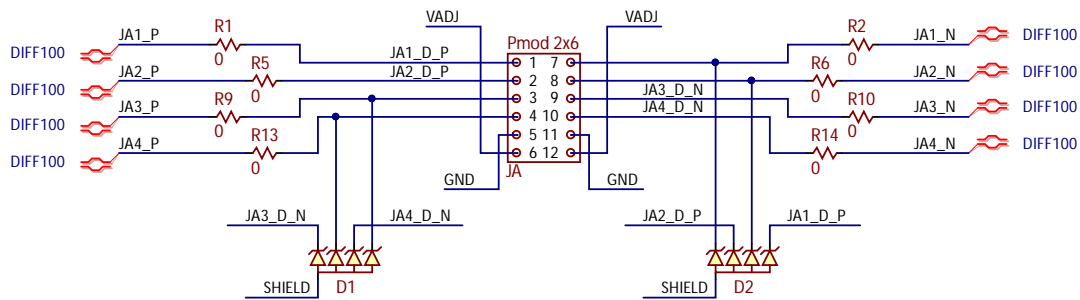
LEGEND:

- = Main Supply Rail Starting Up
Some Time After Power-Up (i.e. from PMU)
- = Aux 3.3VDC Supply Rail Stable
Immediately After Power-Up (i.e. from LDO)

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Circuit I2C Diagram		
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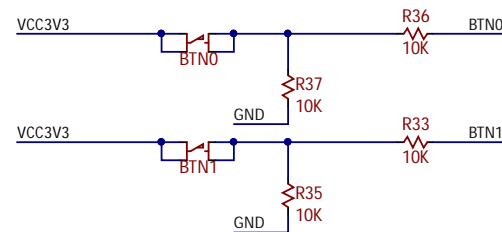
XADC PMOD



MIO LED

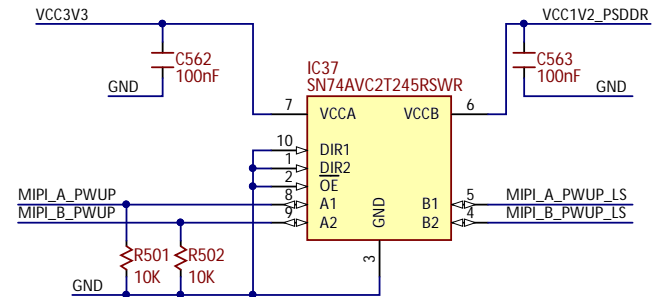
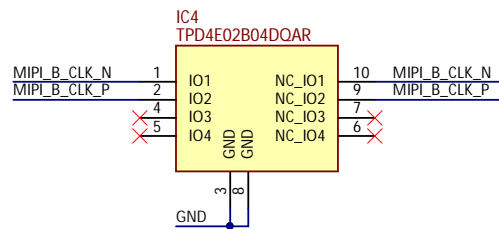
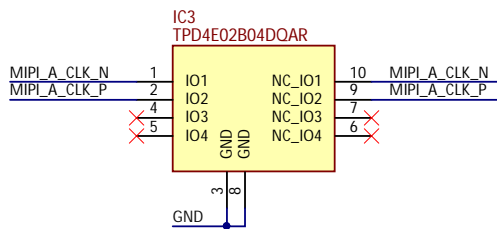
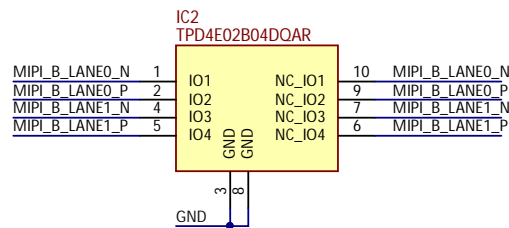
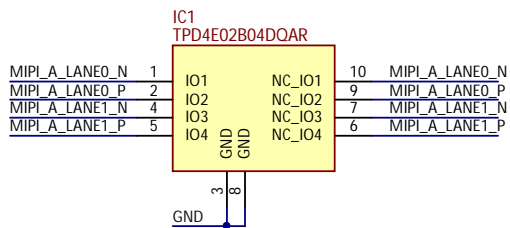
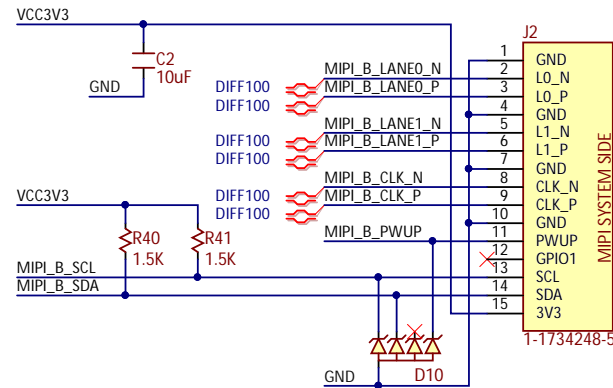
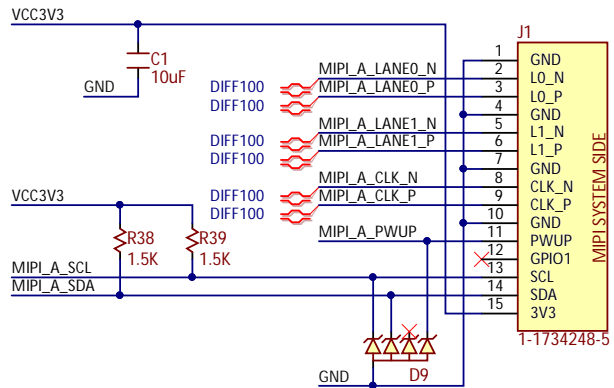


MIO BUTTONS



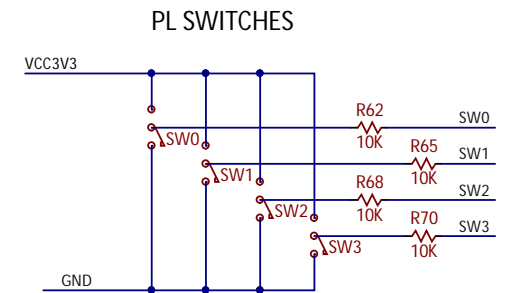
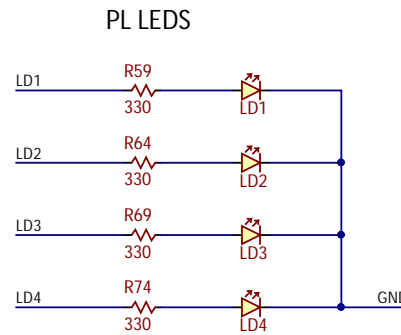
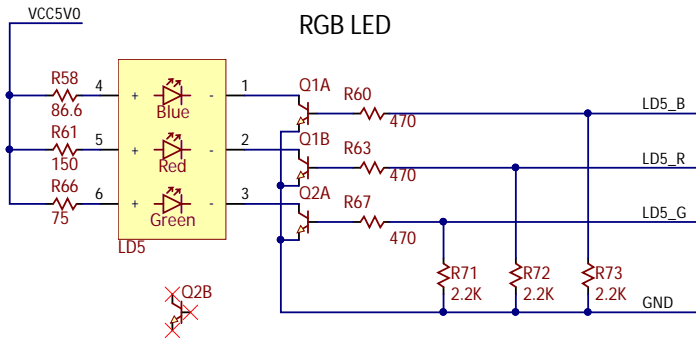
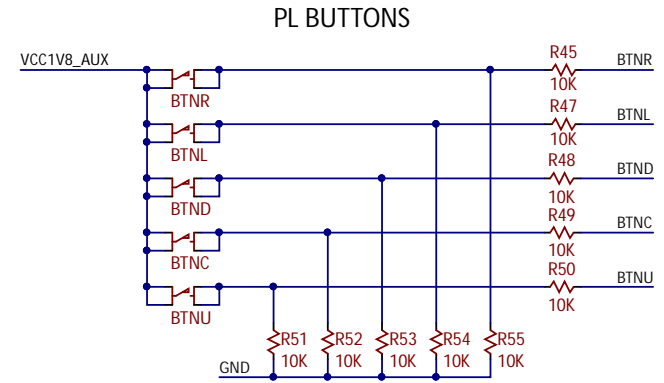
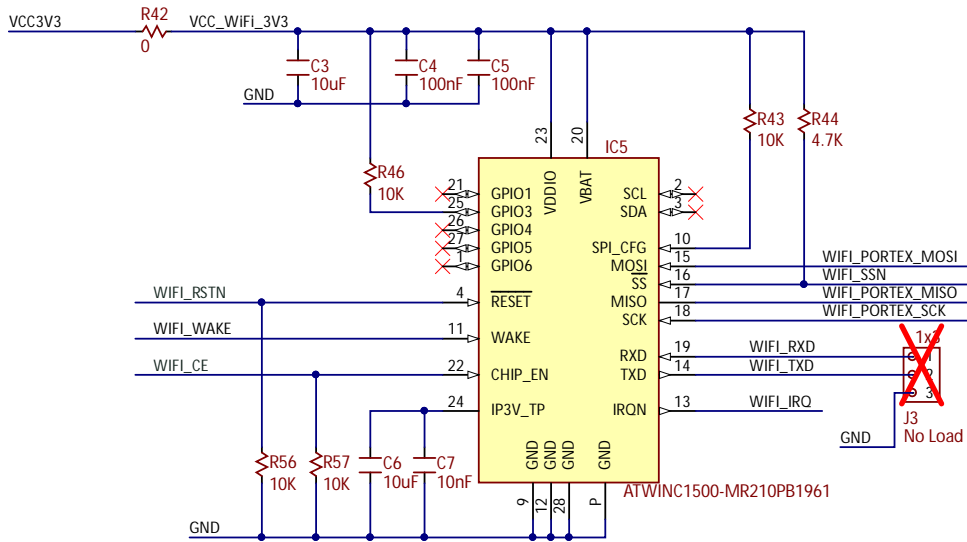
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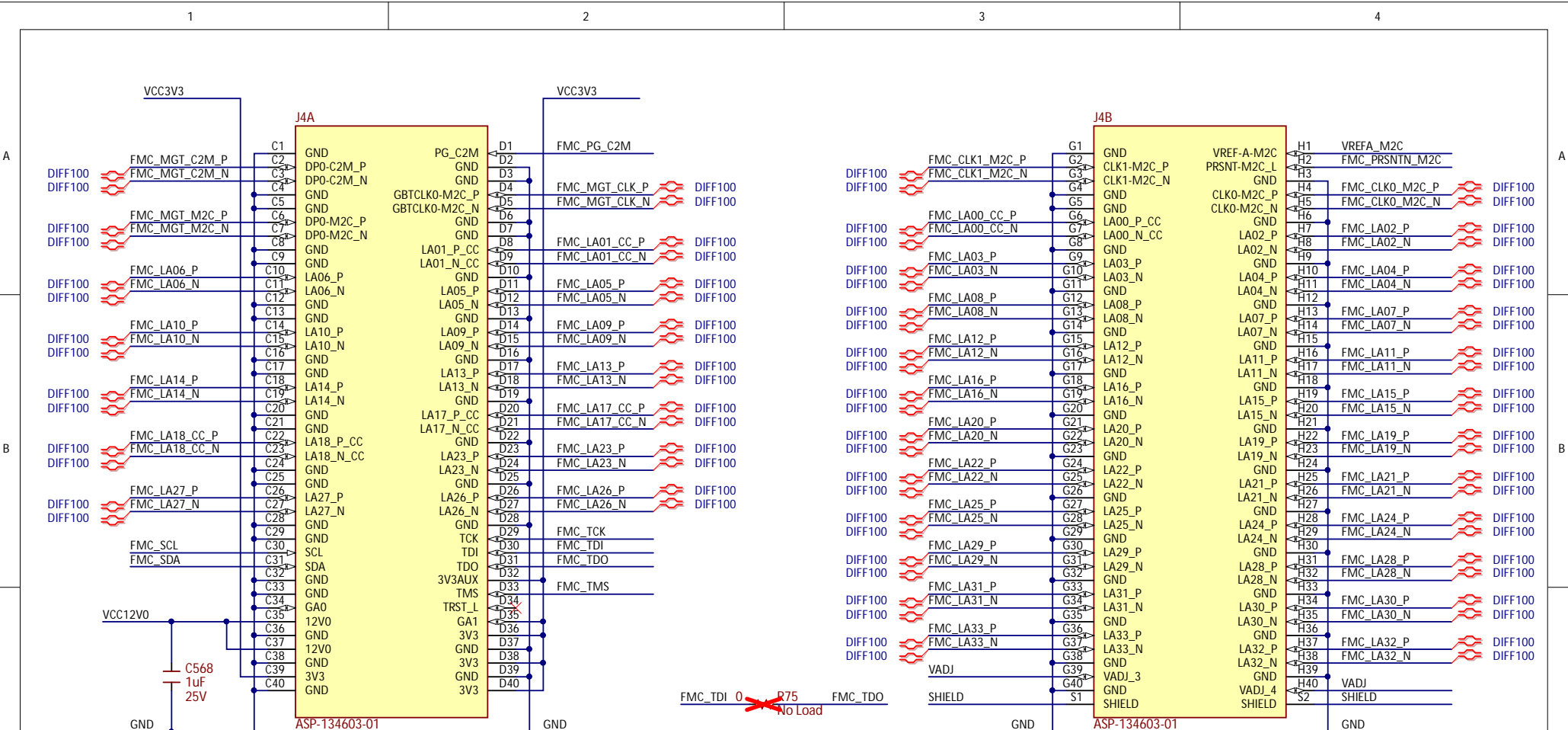
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MIPI Interfaces		
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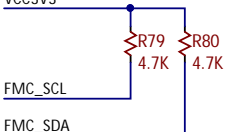
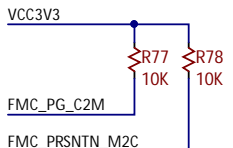
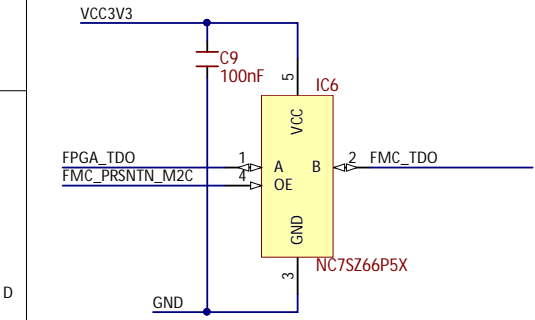
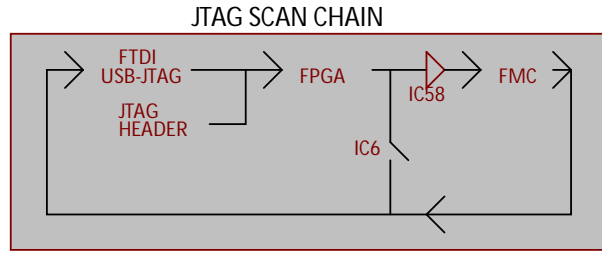


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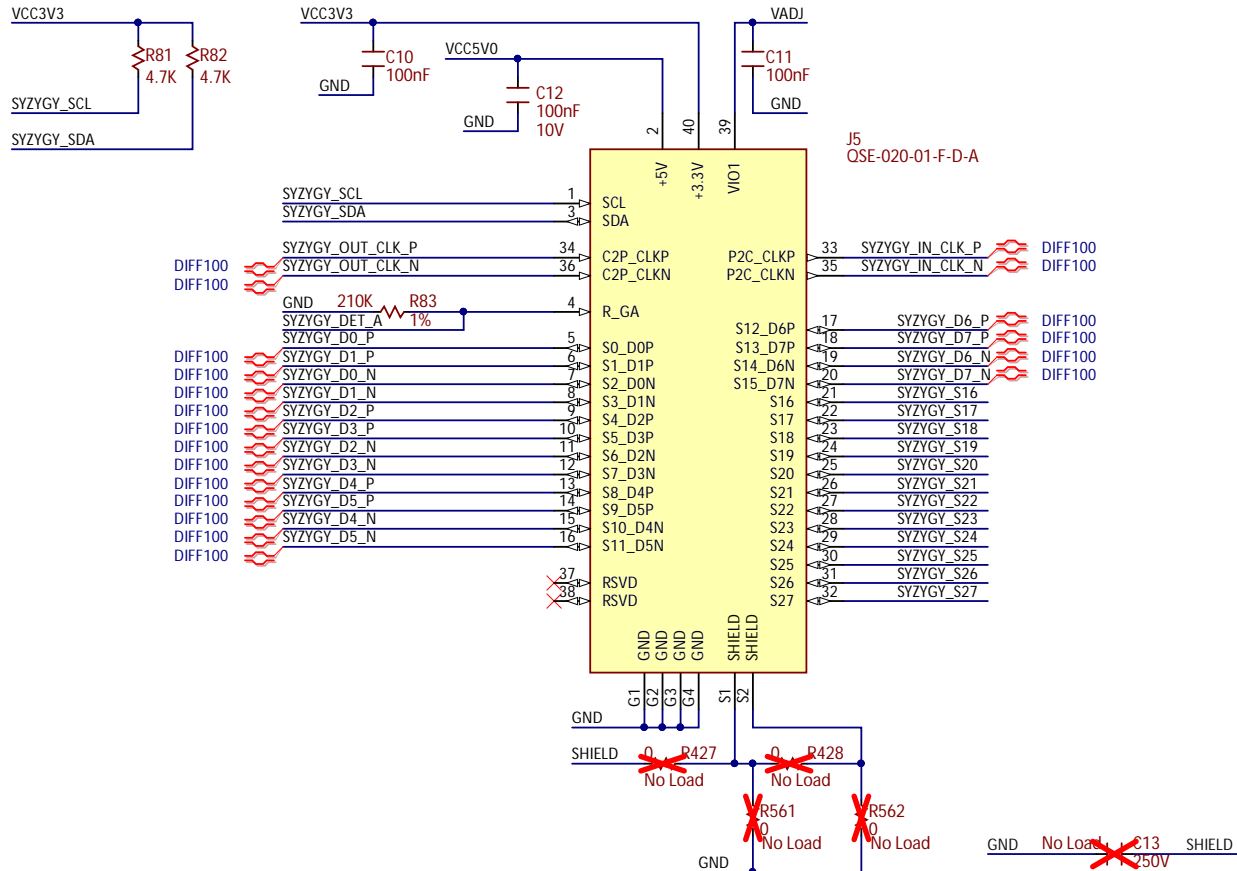


I2C 7-bit addresses ending with bits 01 (due to GAX pins).
 E.g. FMC module EEPROM 7-bit address will be, in binary: 1010001.



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Genesys ZU-3EG		B.1	
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FMC LPC			
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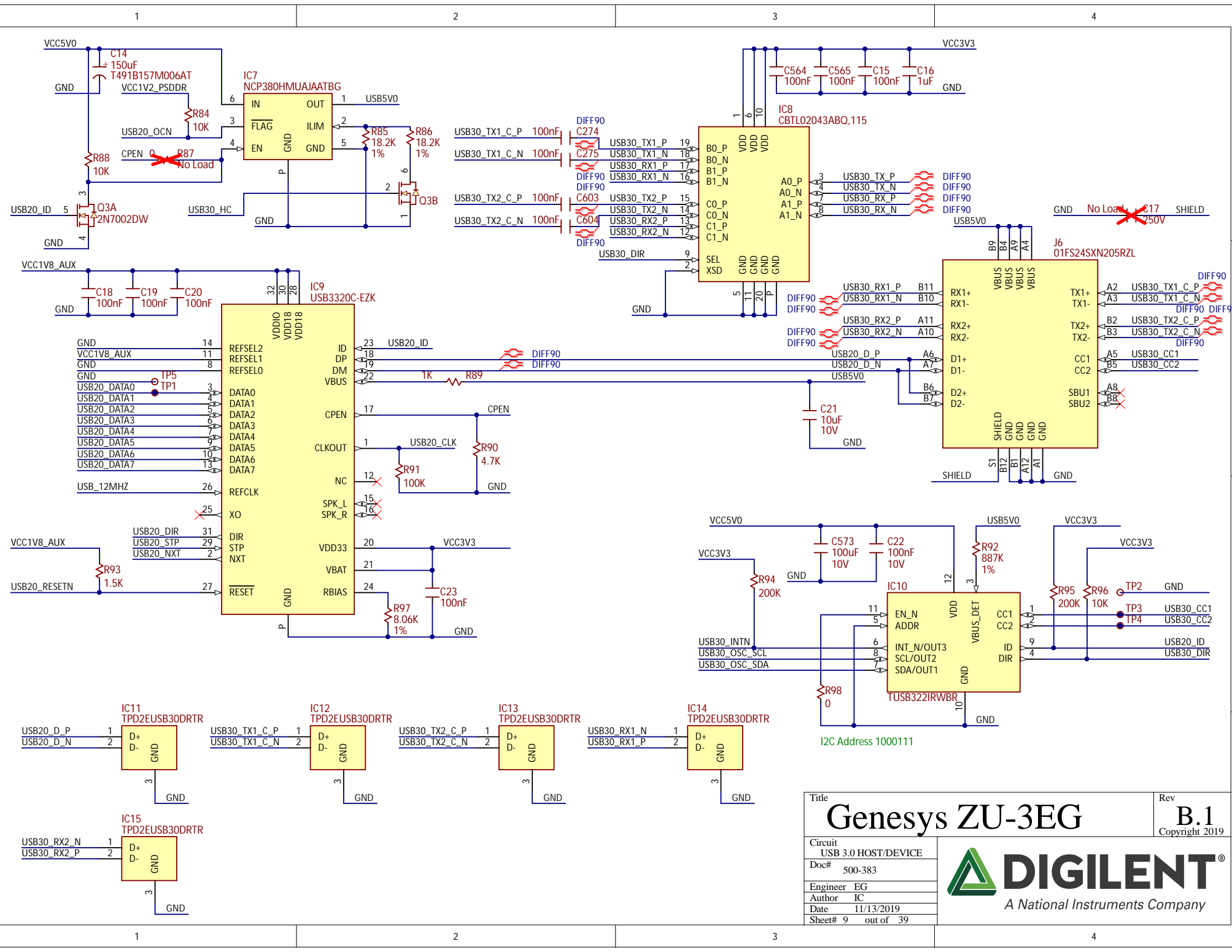




I2C Address 0110000 (due to R_GA)

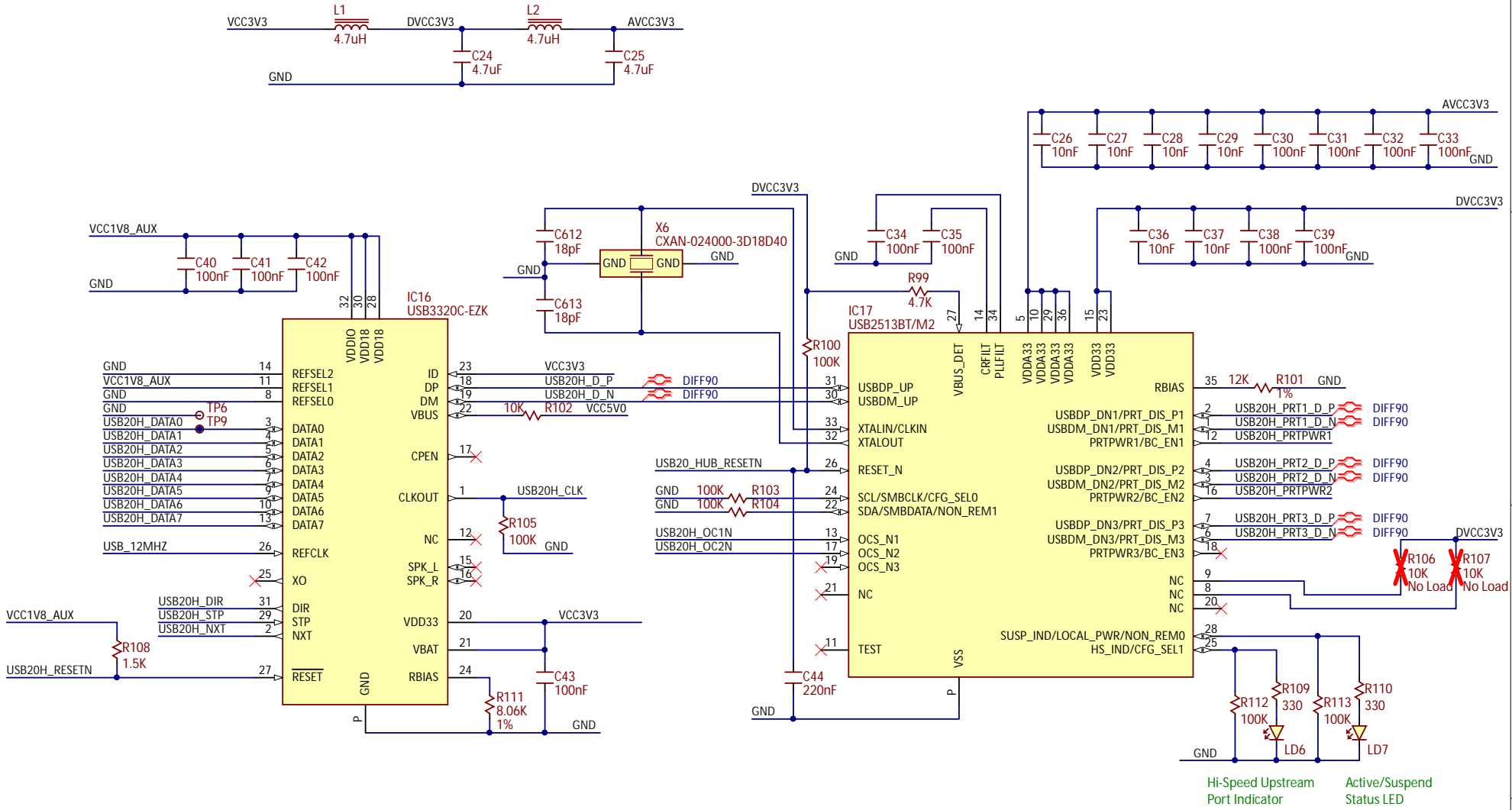
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Circuit		Copyright 2019
SYZYGY Standard Port		
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USB 3.0 HOST/DEVICE		
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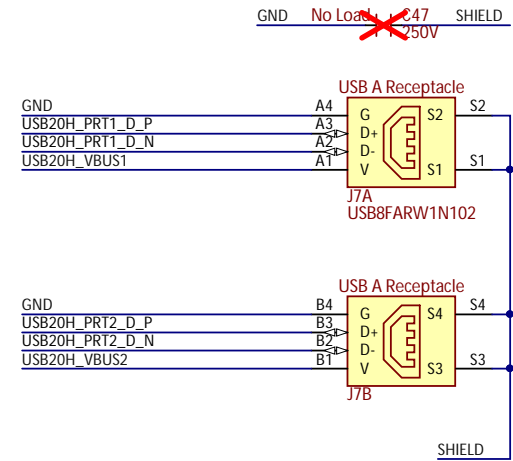
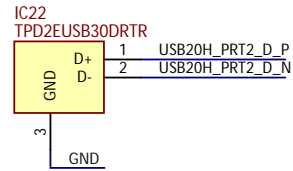
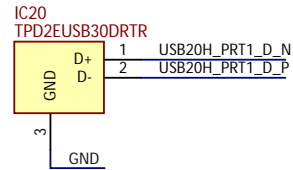
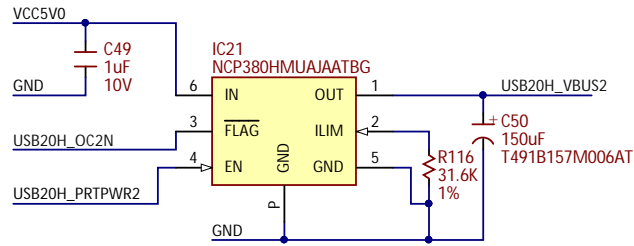
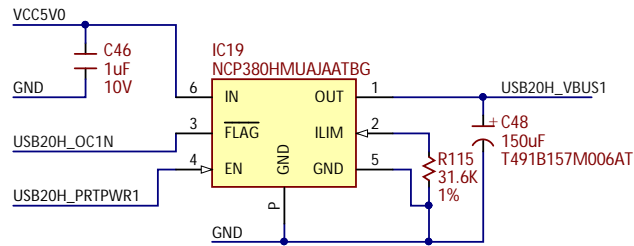




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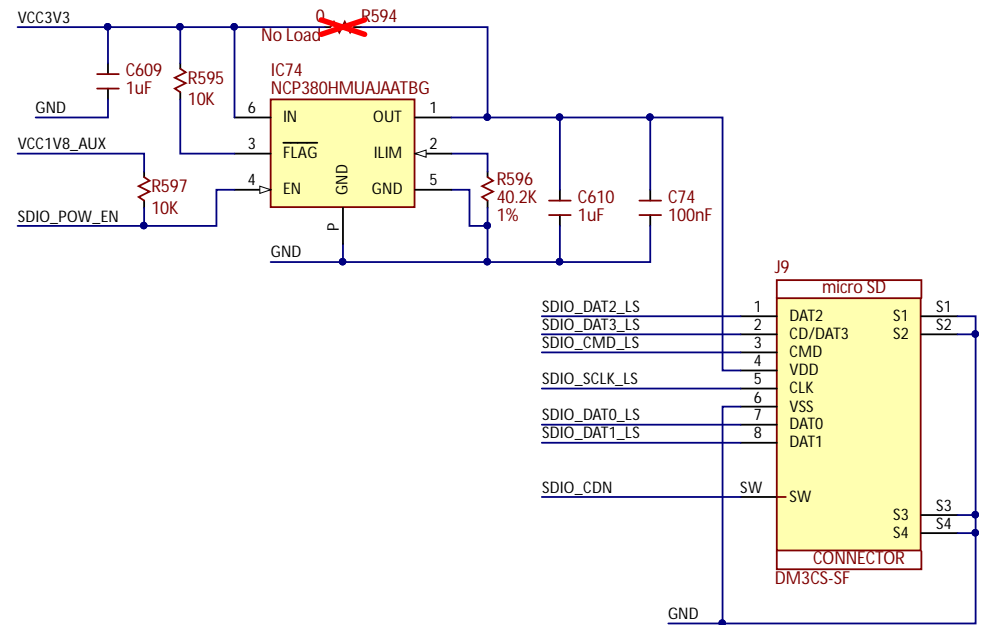
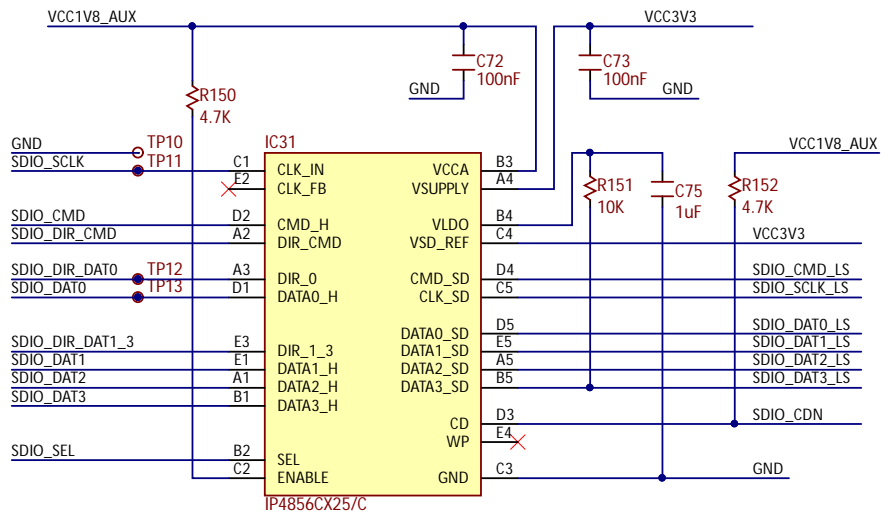
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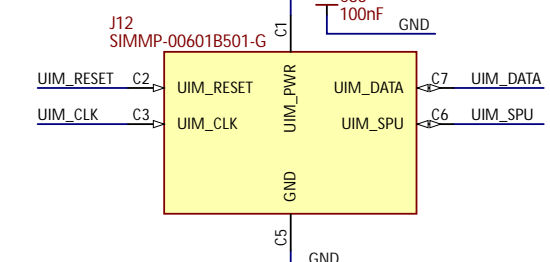
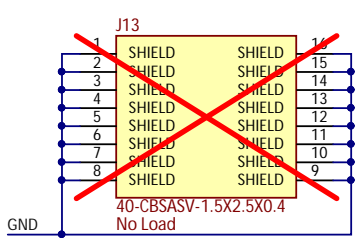
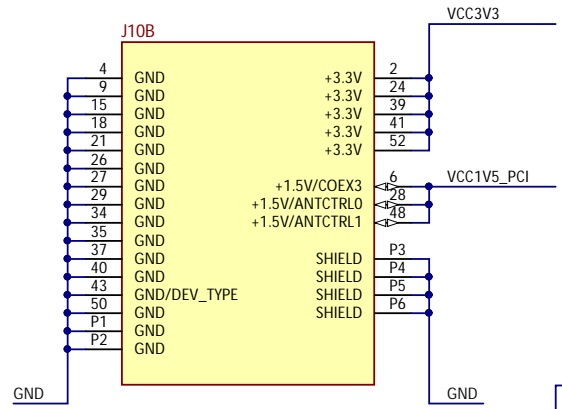
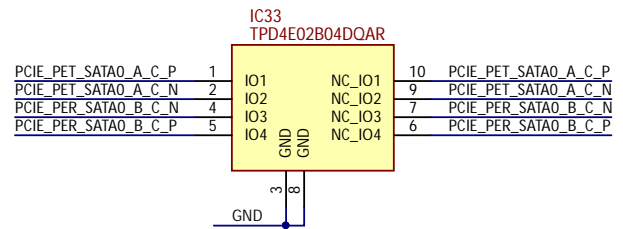
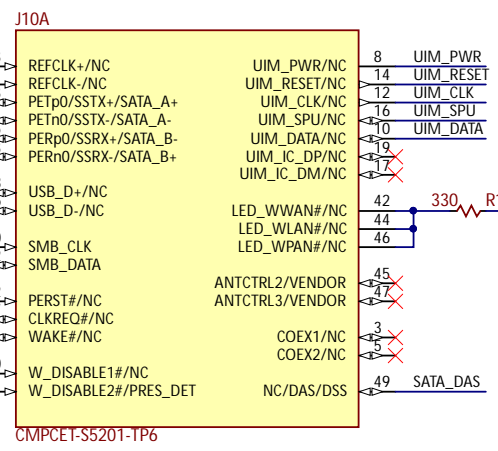
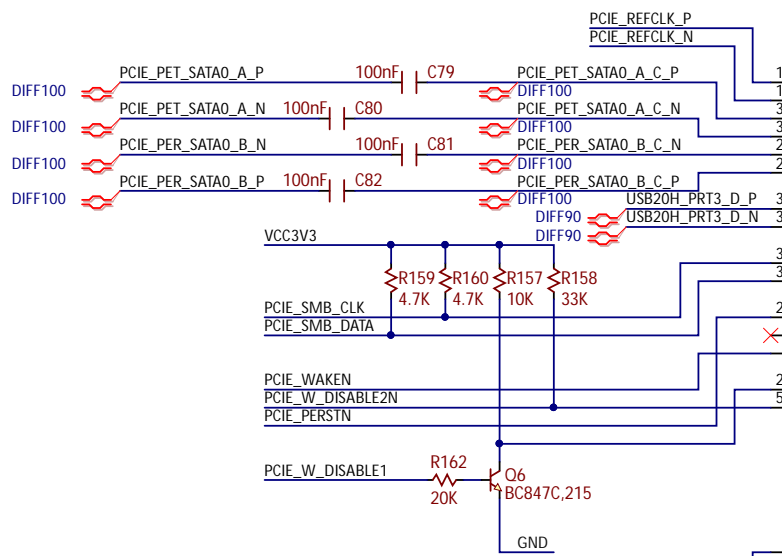
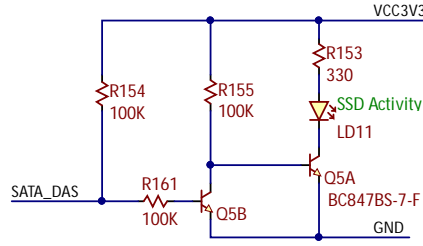
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Circuit	SD CARD	
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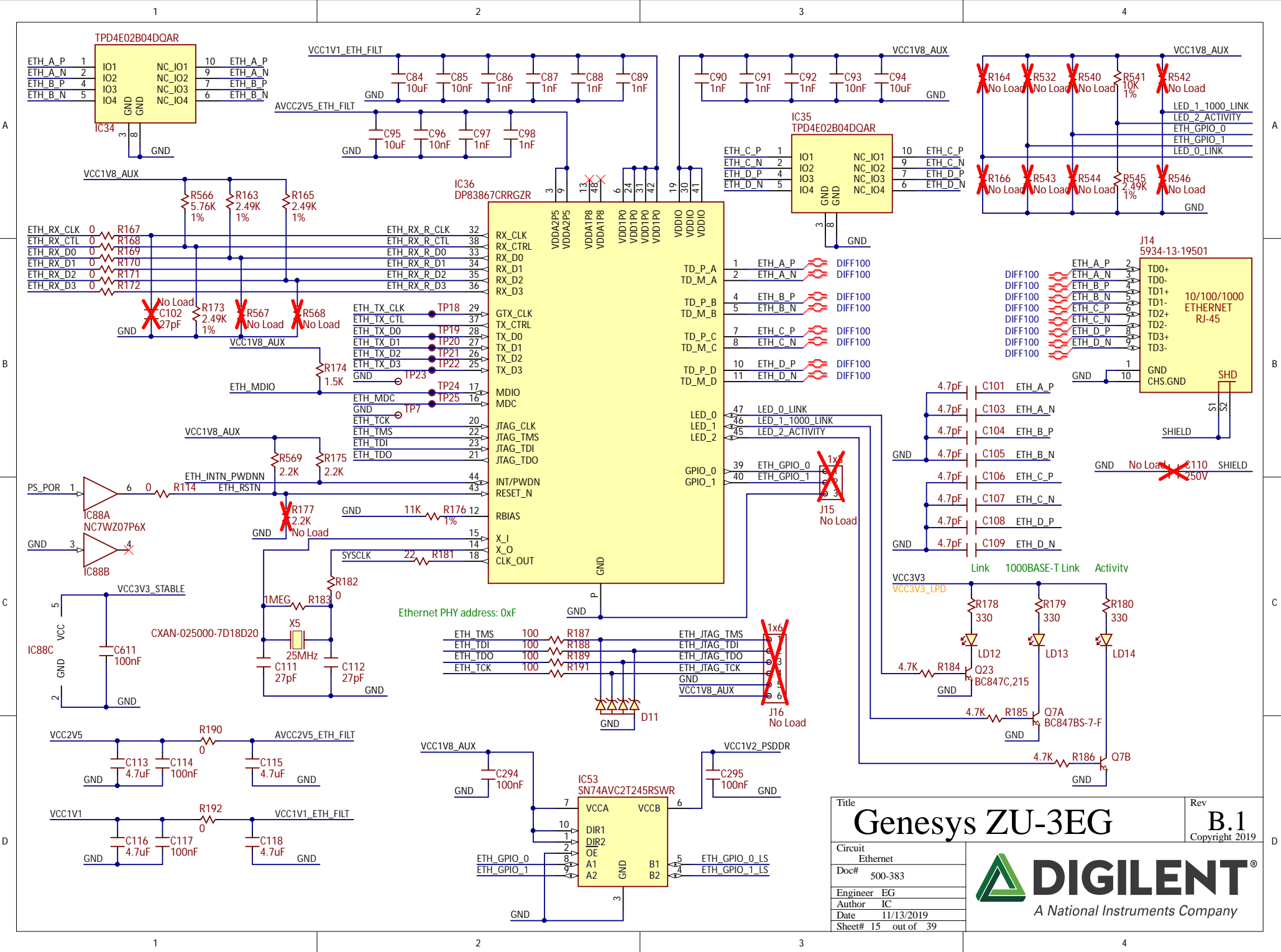
Wireless Activity

~~J42 SMA No Load~~

~~J11 SMA No Load~~

- F11 SMT Standoff S001-00001-B01
- F12 SMT Standoff S001-00001-B01
- F13 mini PCIe Screw I02003MN
- F14 SMT Standoff S001-00001-B01
- F15 SMT Standoff S001-00001-B01
- F16 mini PCIe Screw I02003MN
- F17 M-F Standoff RE025MN01
- F18 M-F Standoff RE025MN01

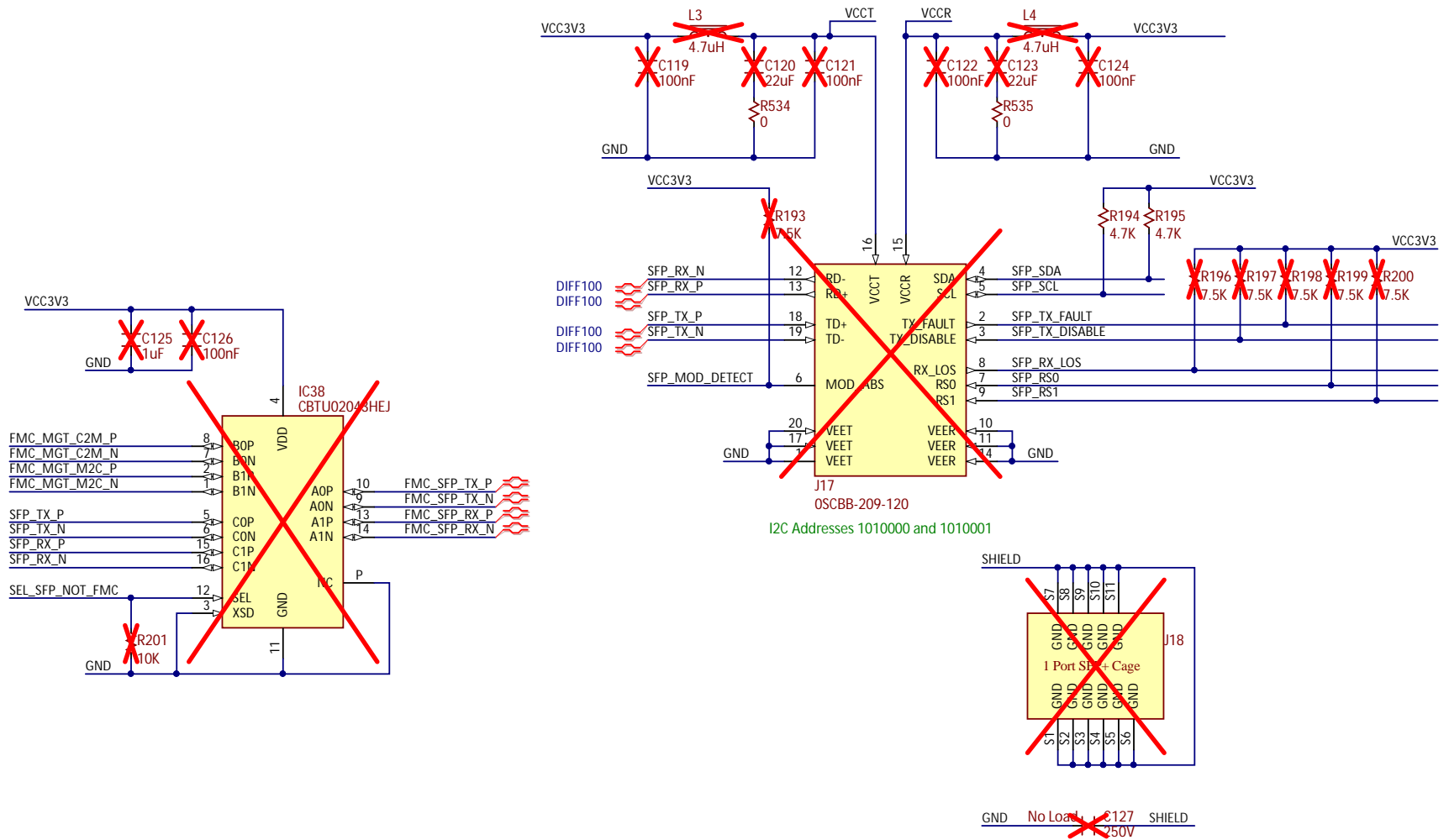
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Circuit		Copyright 2019	
Mini PCIe / SATA			
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Ethernet			
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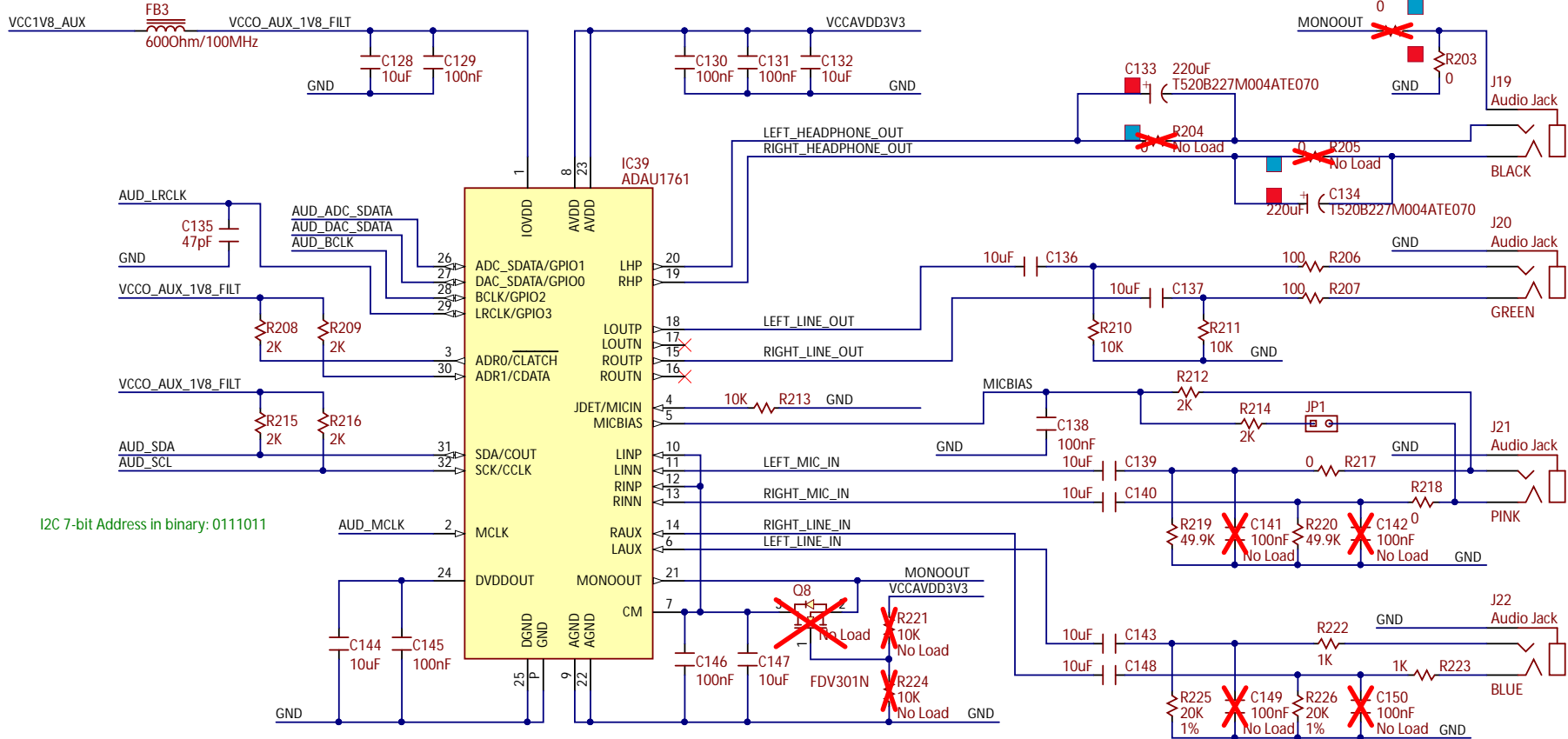
SFP+ cannot be used simultaneously with neither HDMI Source nor Sink due to the limited number of QPLL/CPLL primitives available in the GTH Quad.

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Genesys ZU-3EG		B.1
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Circuit	SFP+	
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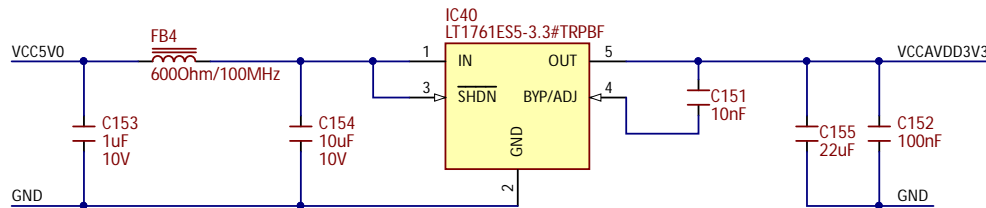


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NOTE: Load No Load
 Capless Headphone ■ ■
 AC-Coupled Headphone ■ ■

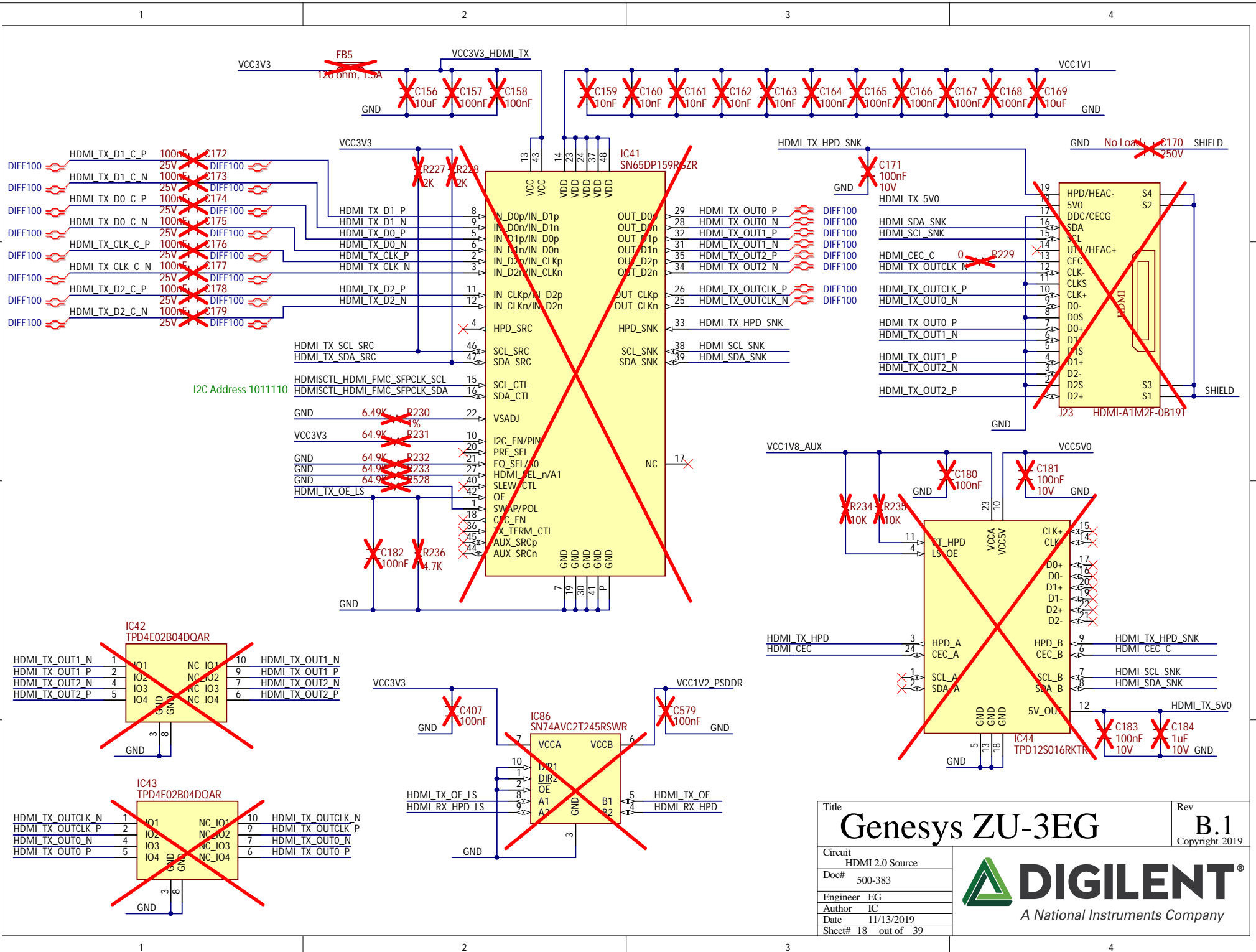


I2C 7-bit Address in binary: 0111011



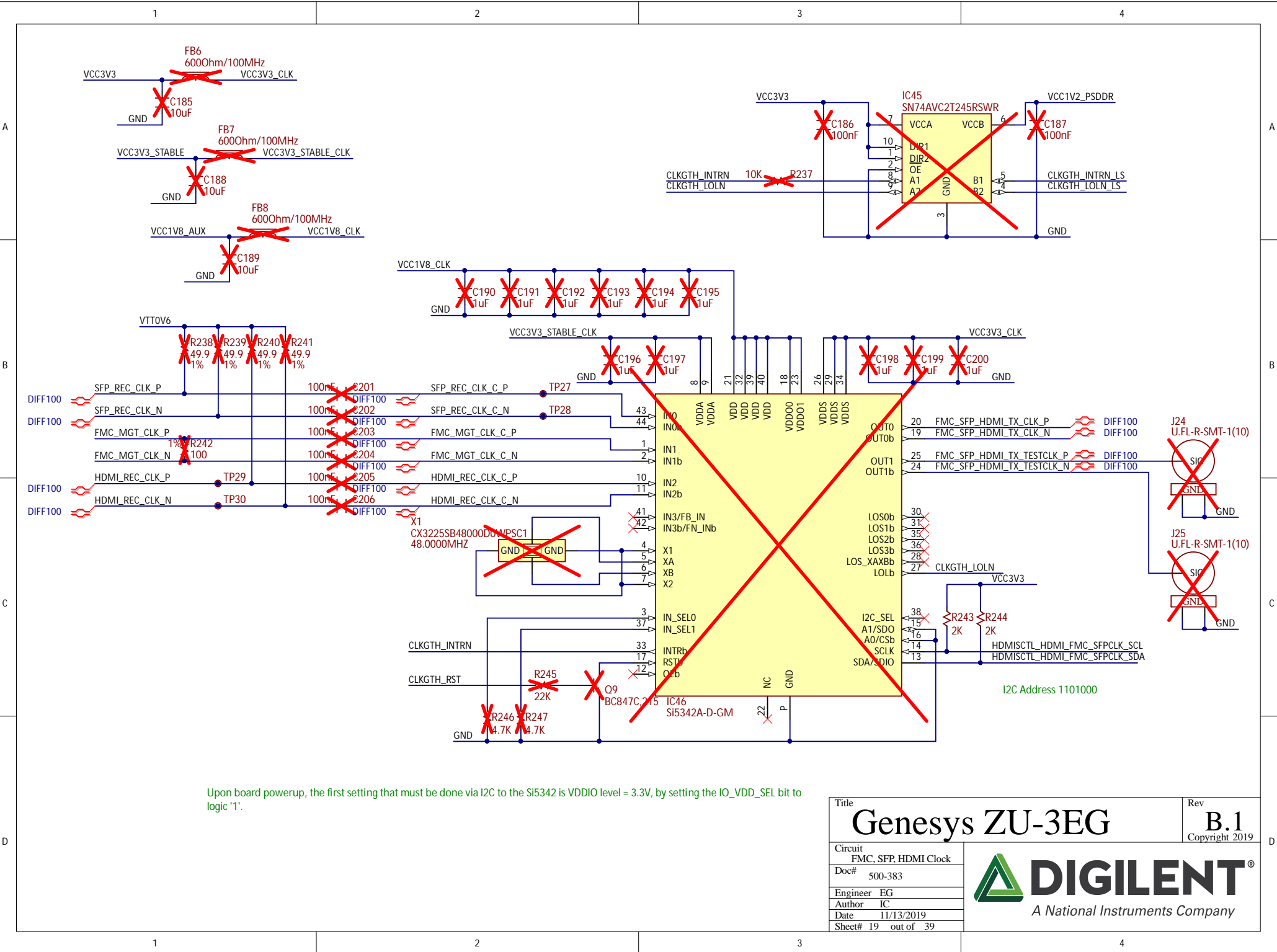
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Circuit	AUDIO	
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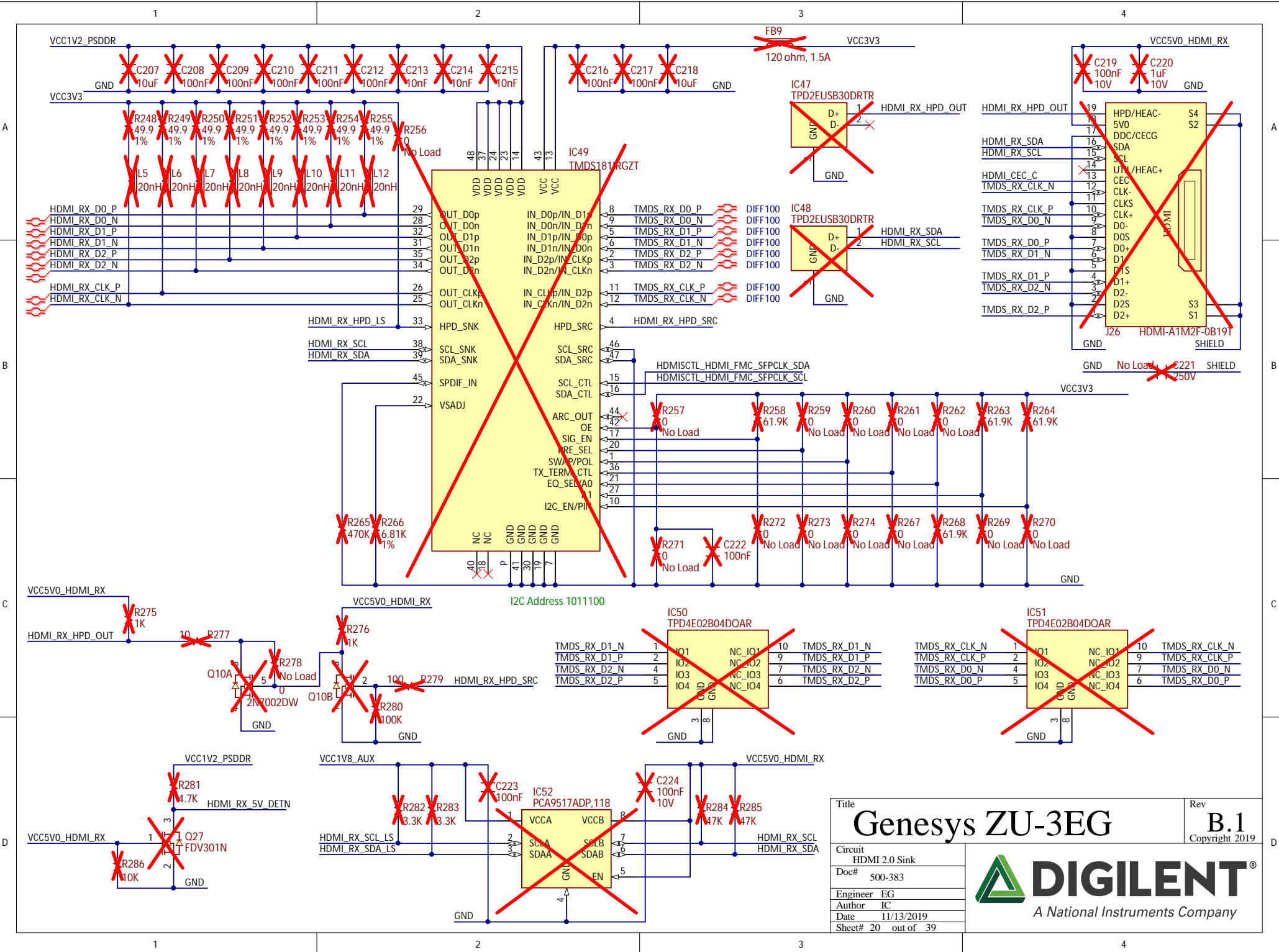
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Circuit		Copyright 2019	
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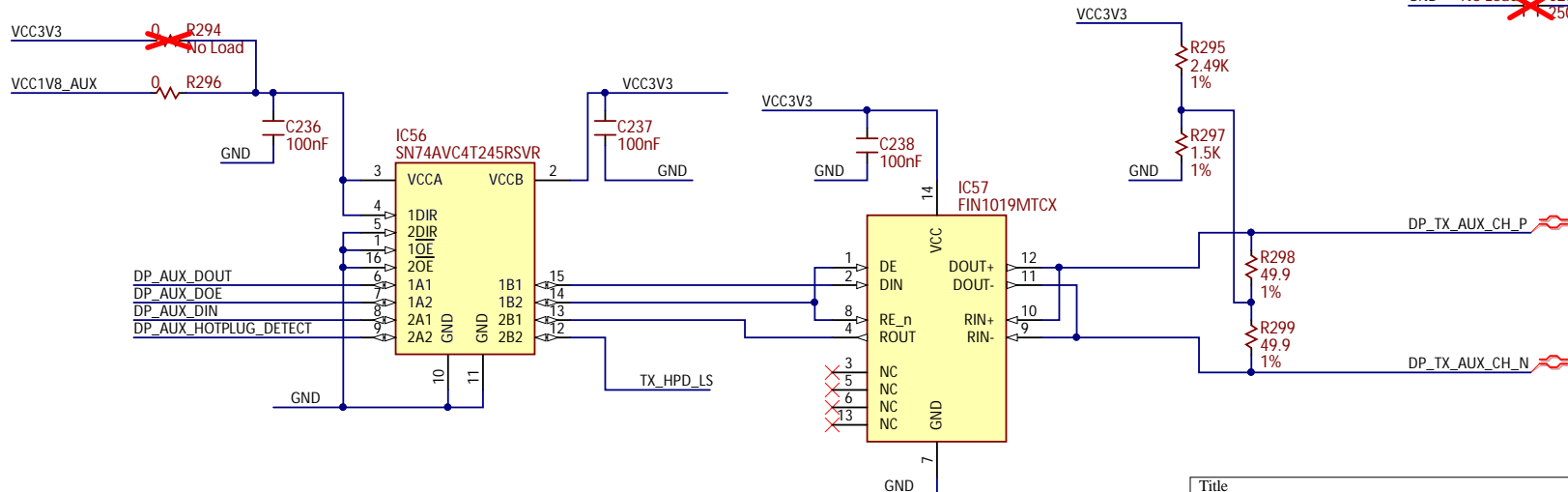
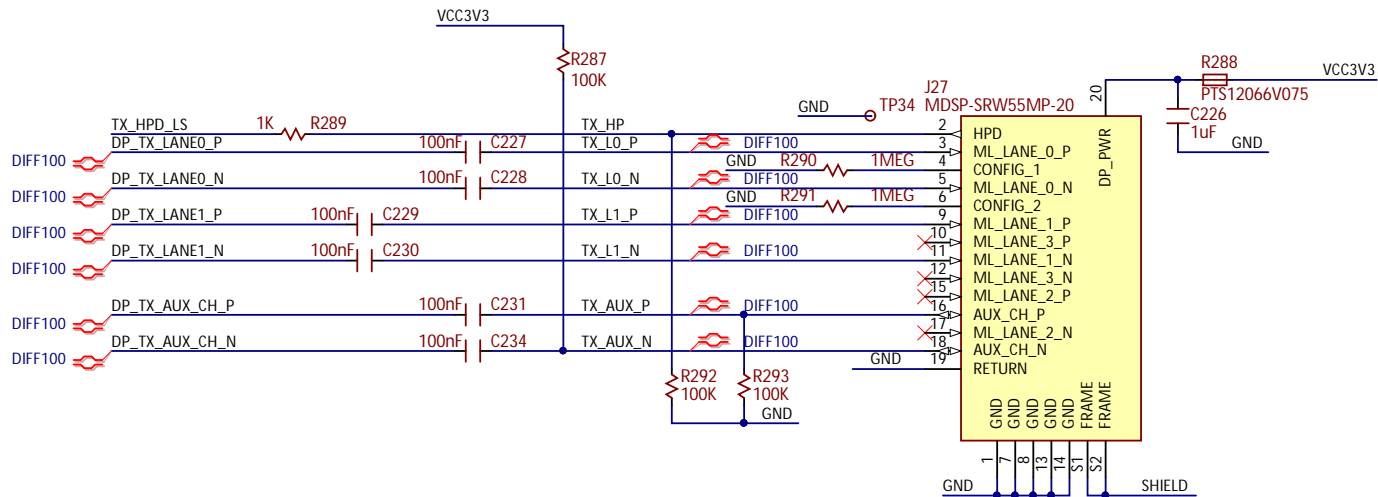
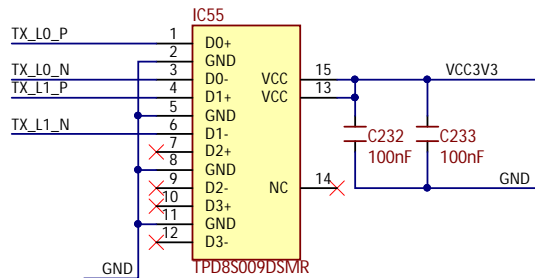
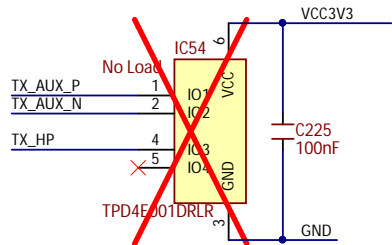
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Circuit		Copyright 2019
FMC, SFP, HDMI Clock		
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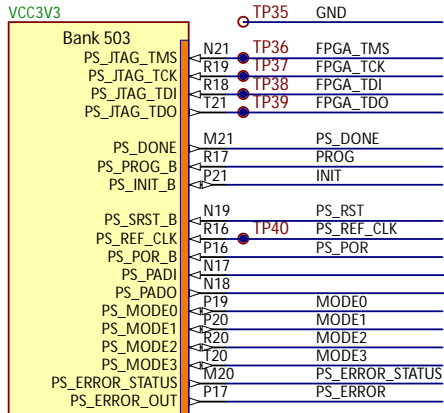
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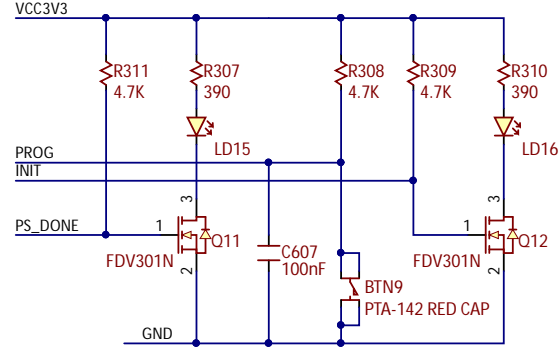
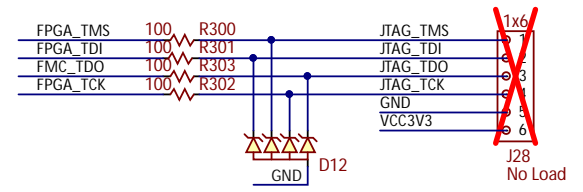
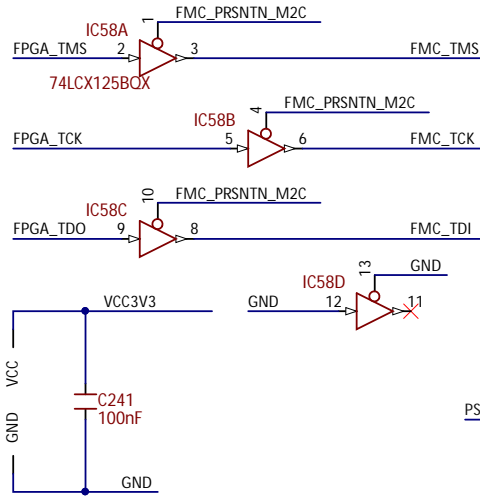


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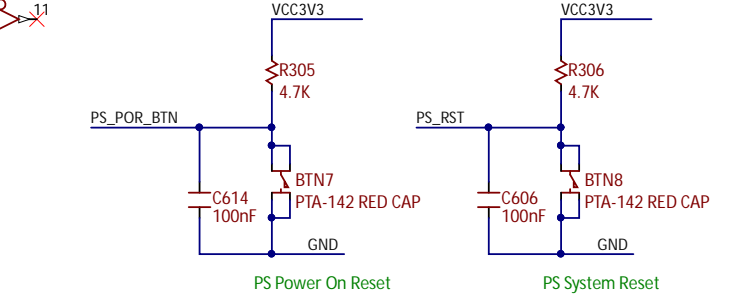
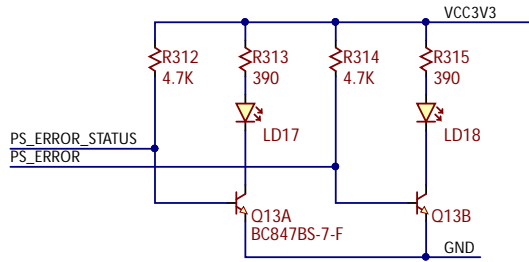




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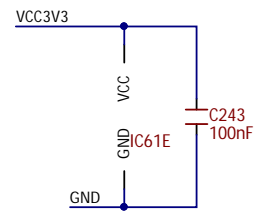
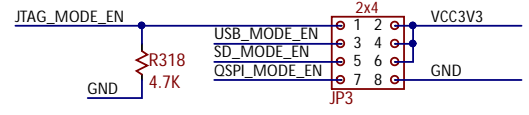
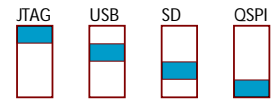
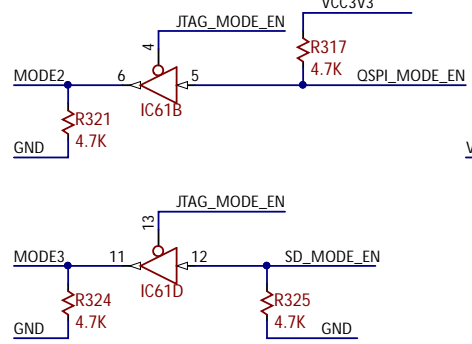
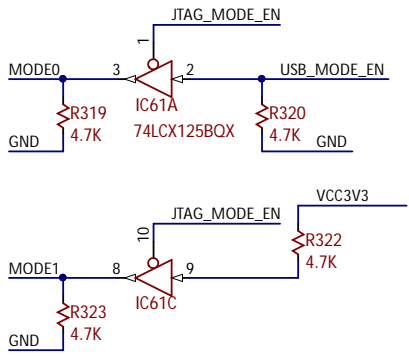
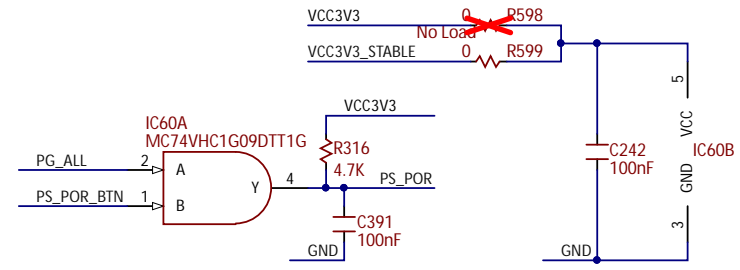


PL Configuration Reset

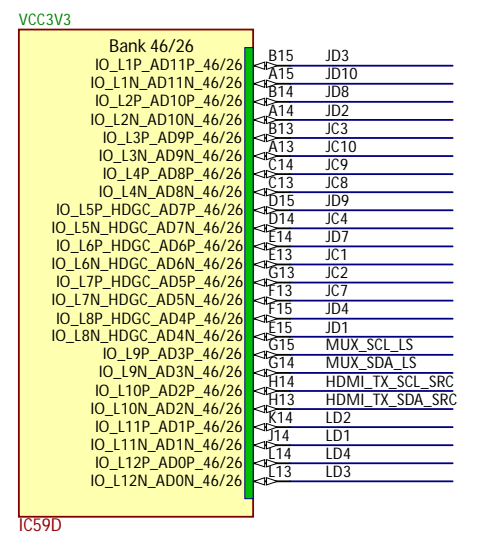
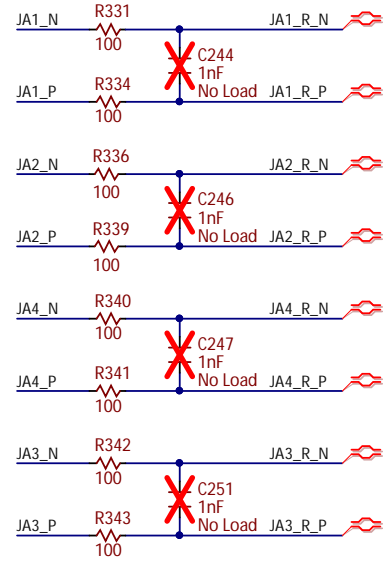
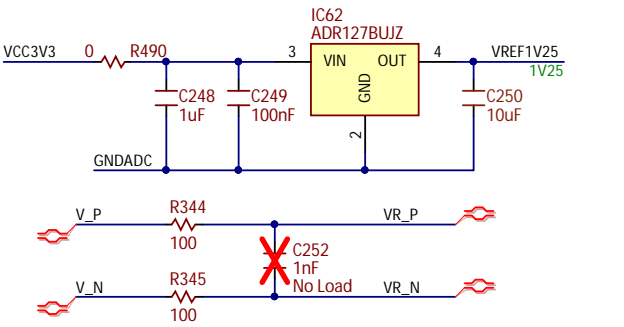
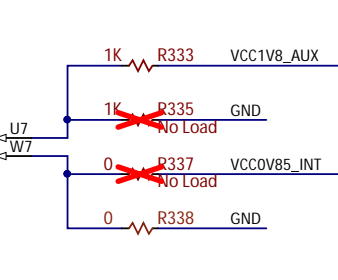
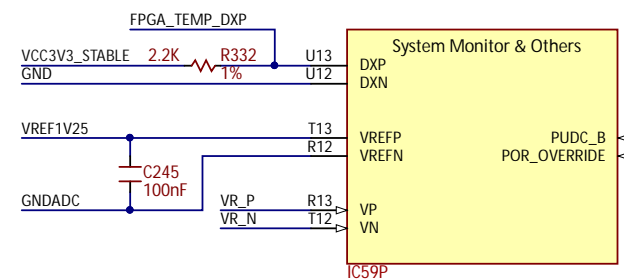
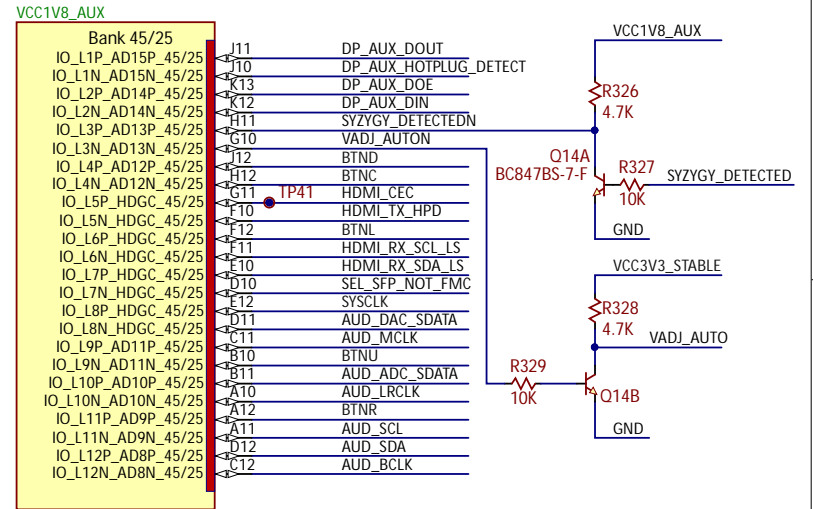
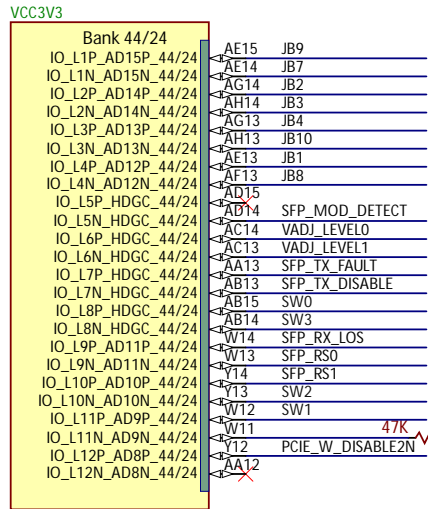
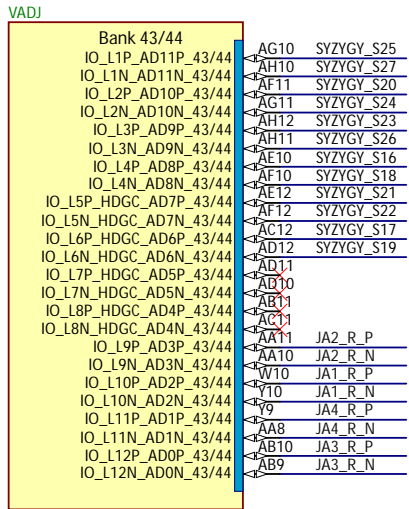


PS Power On Reset

PS System Reset



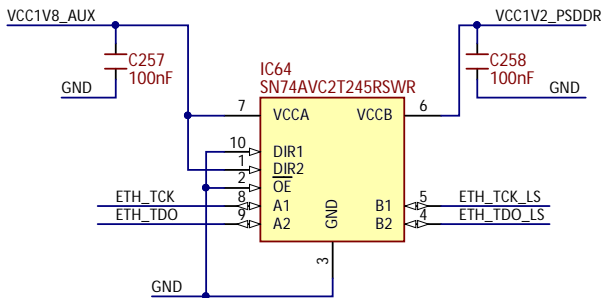
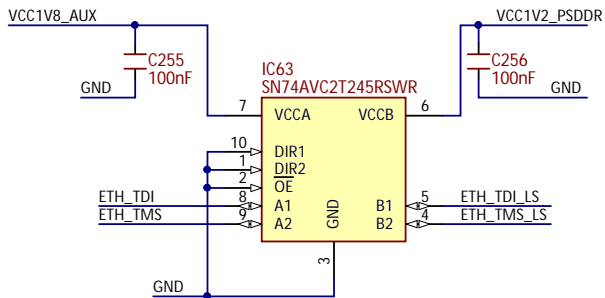
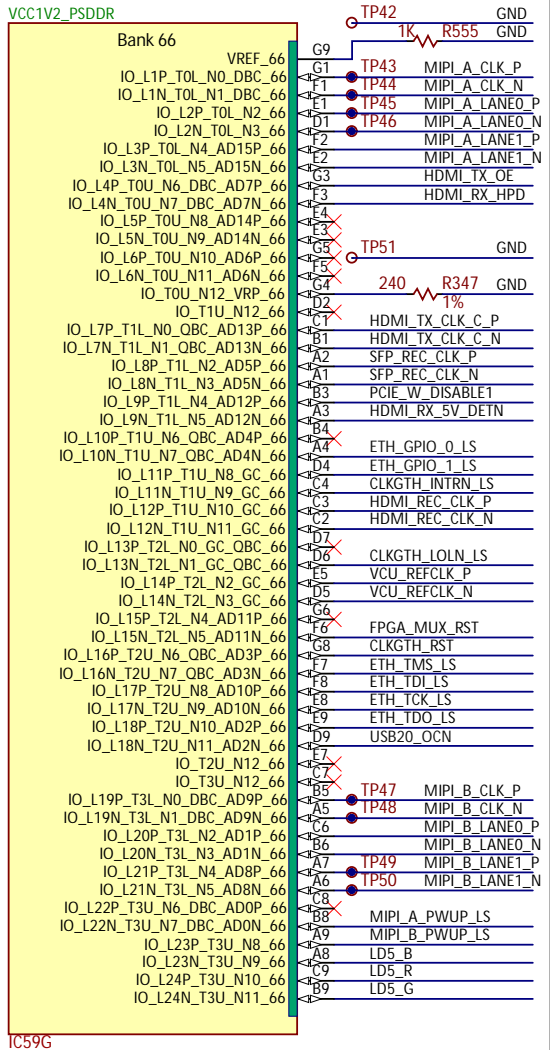
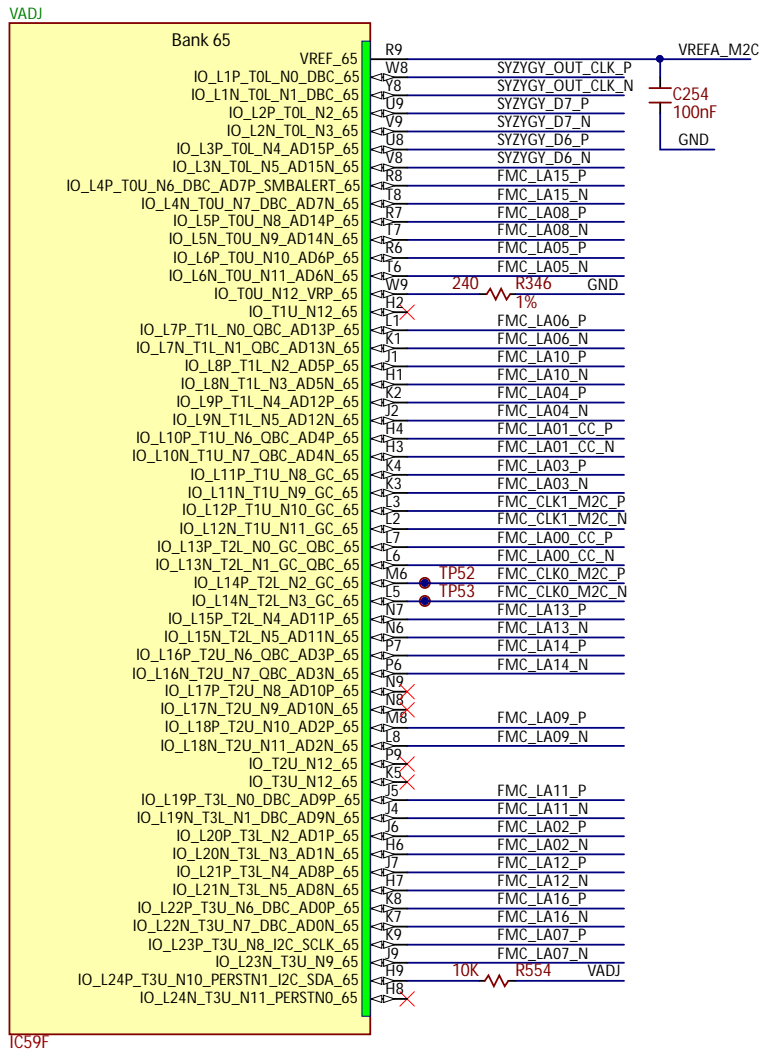
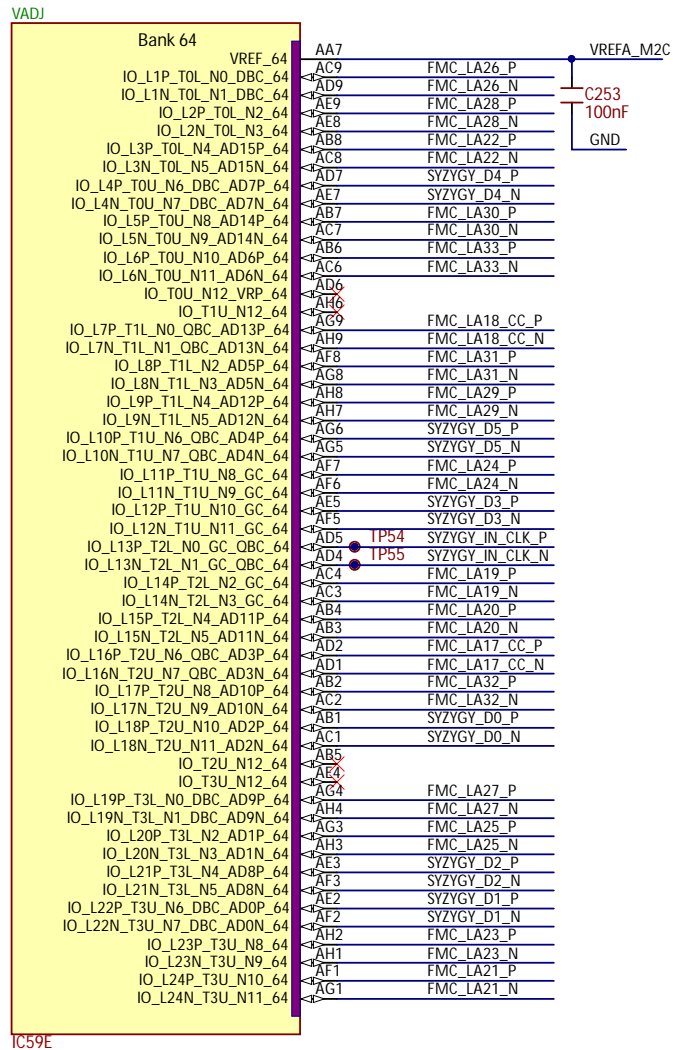
Title		Rev	
Genesys ZU-3EG		B.1	
Circuit		Copyright 2019	
FPGA CONFIG			
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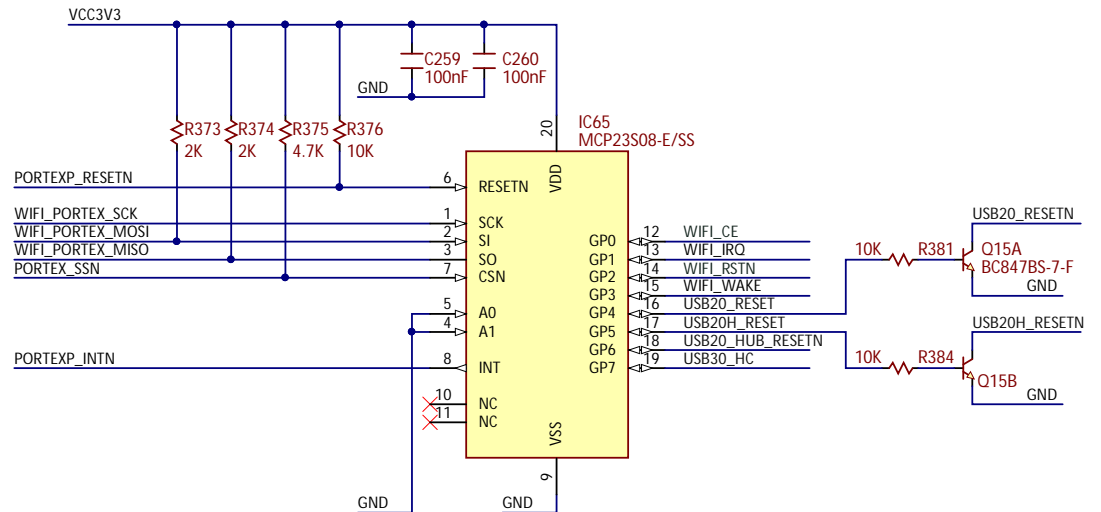
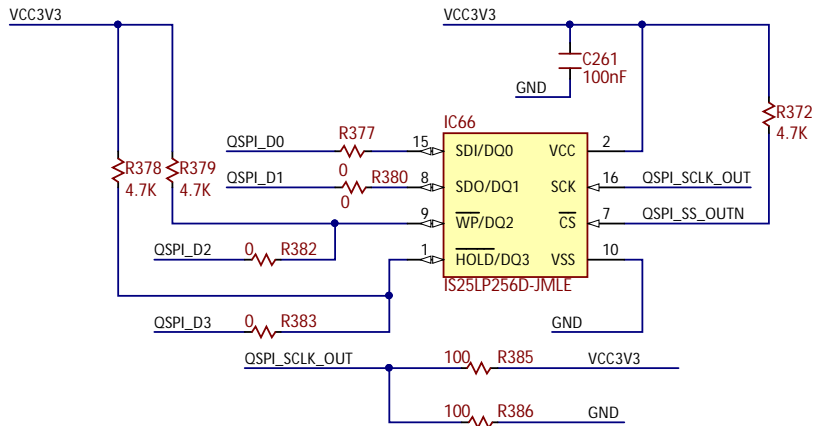
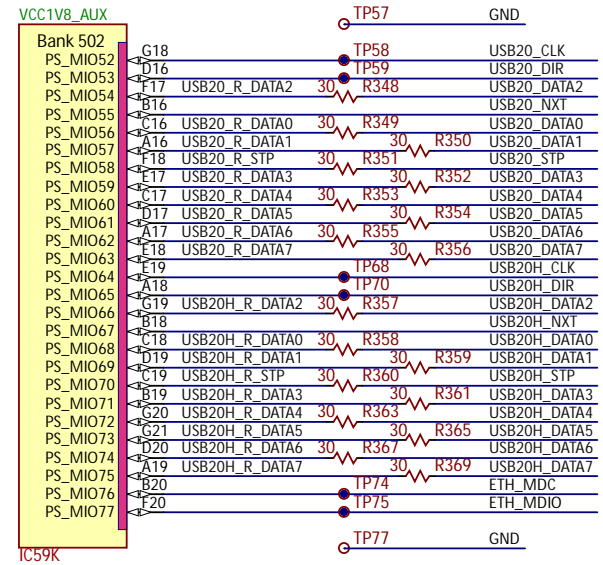
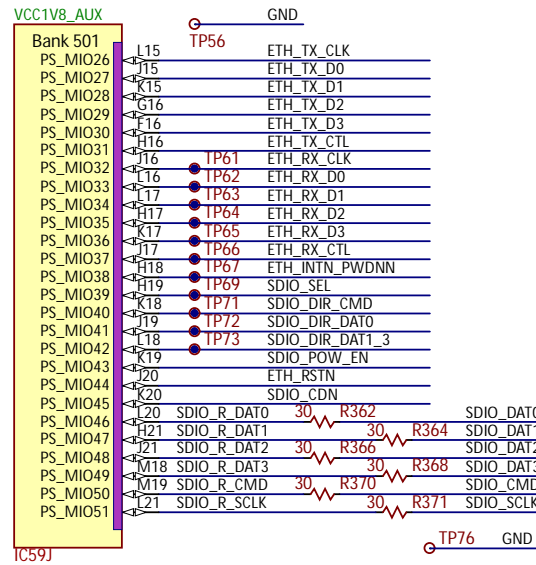
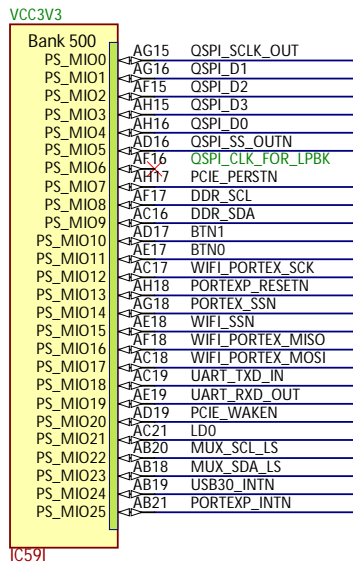


If a DCI standard is required on FMC_LA15_P and/or FMC_LA07_P, follow the requirements outlined in UG571, under section "Special DCI Requirements in Some Banks".

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	Copyright 2019
Circuit	HP FPGA BANKS
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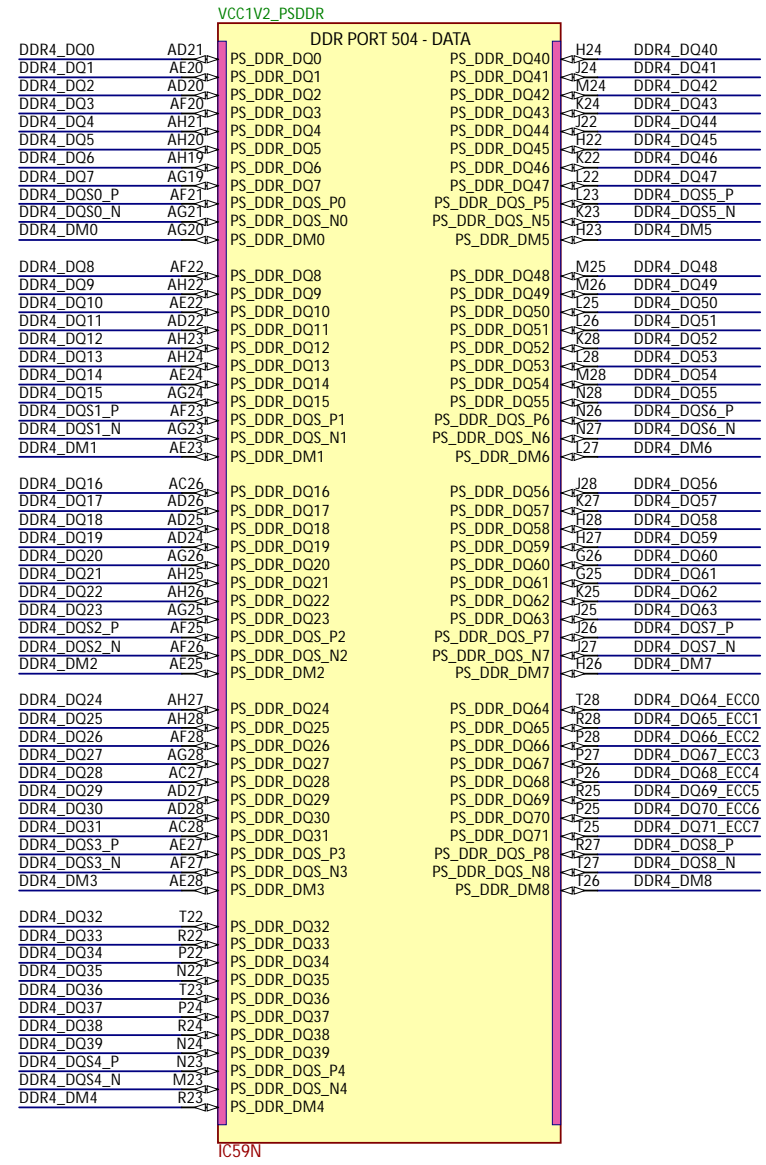
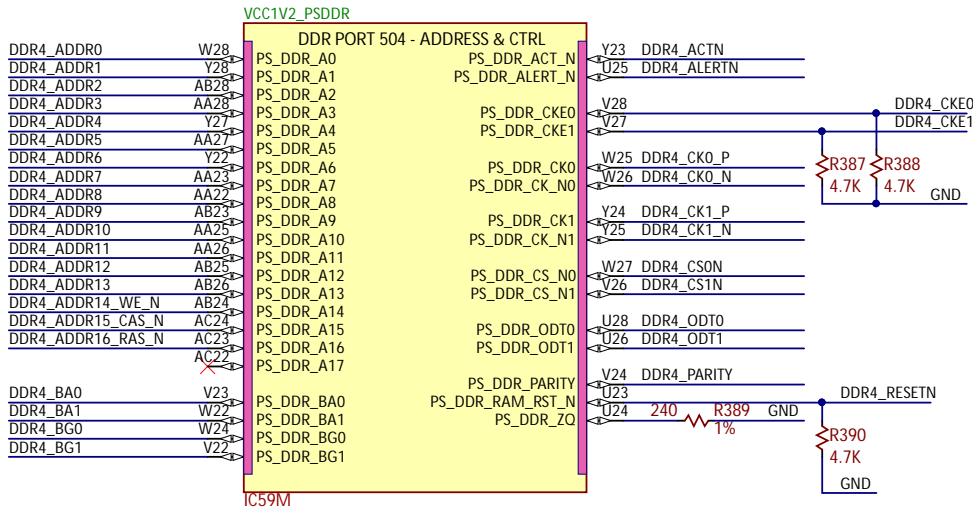
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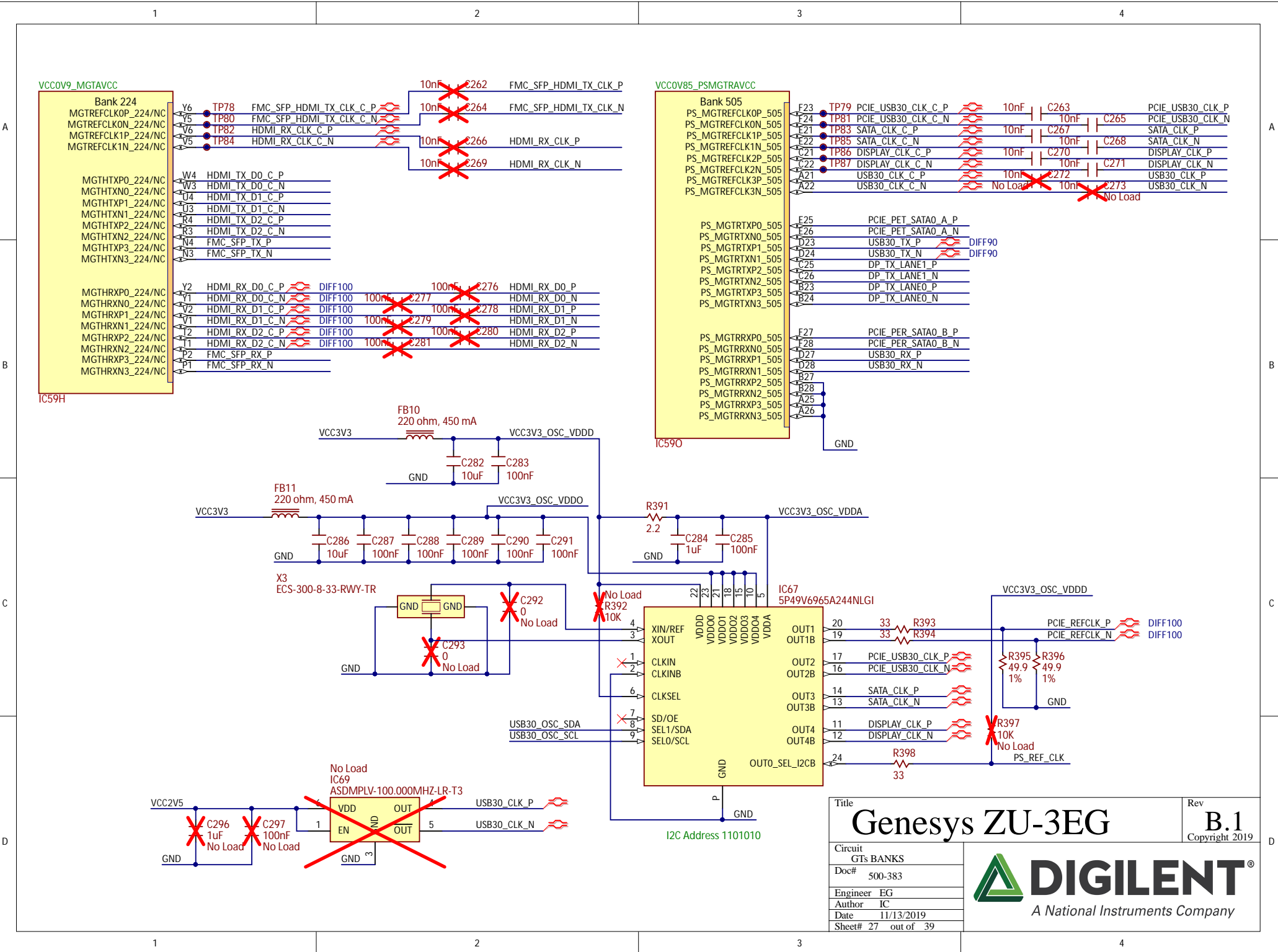
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			Copyright 2019
Circuit	MIO BANKS; SPI FLASH		
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GTs BANKS			
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A

B

C

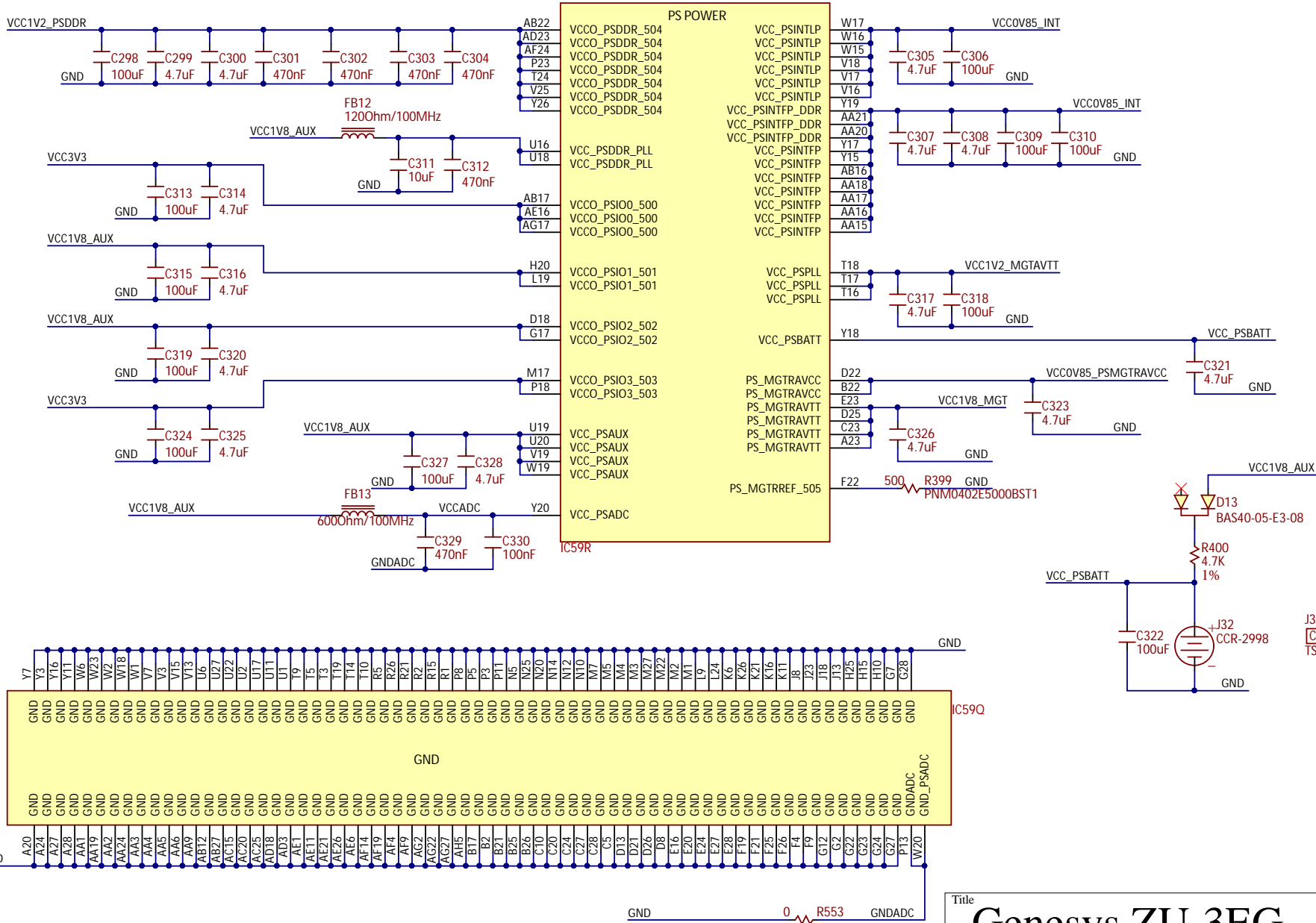
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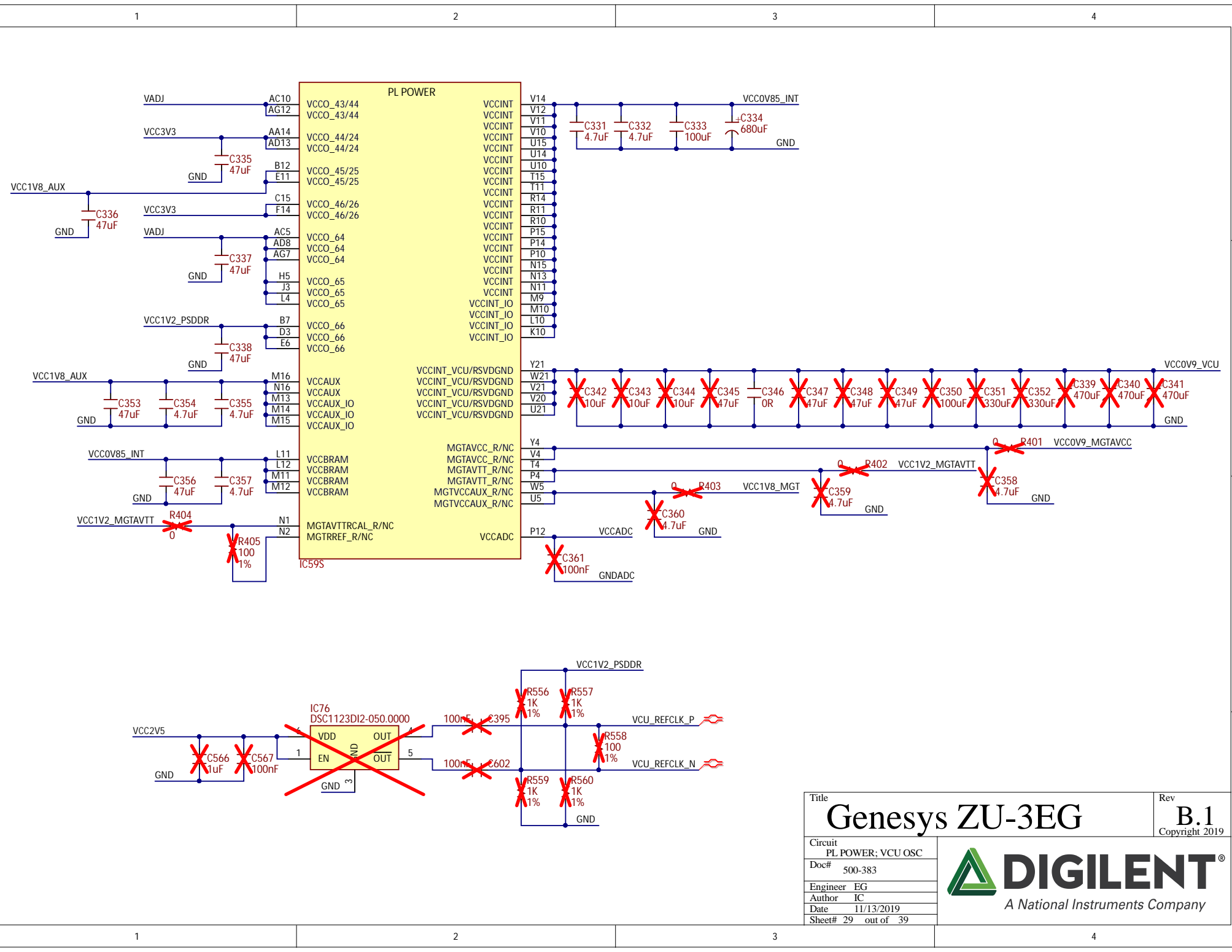
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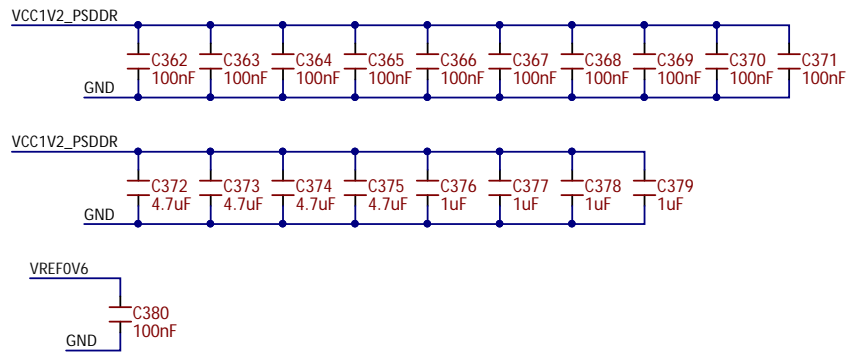
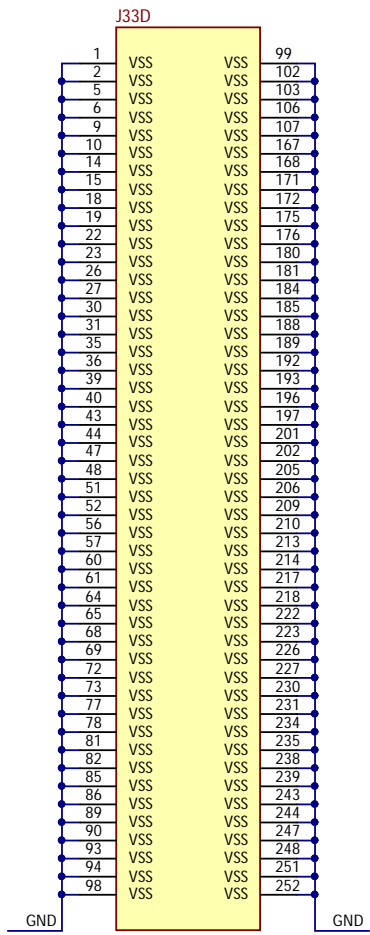
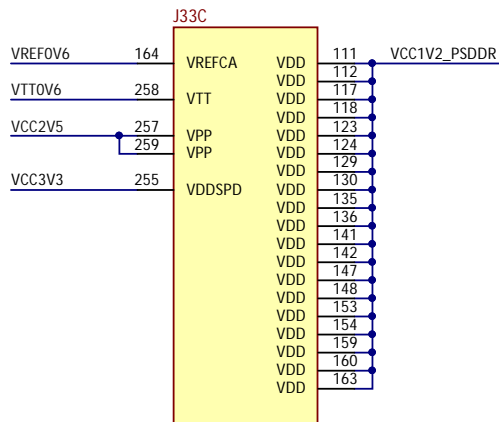


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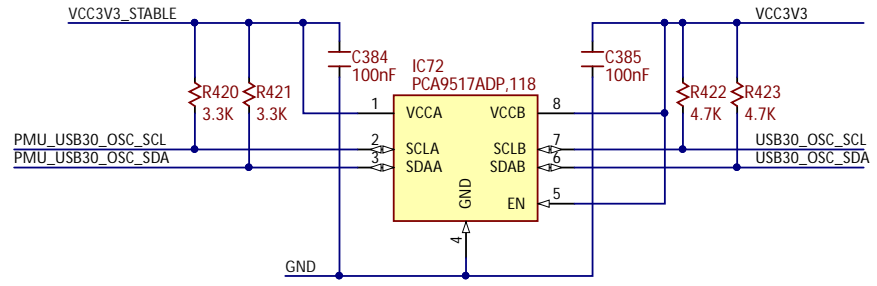
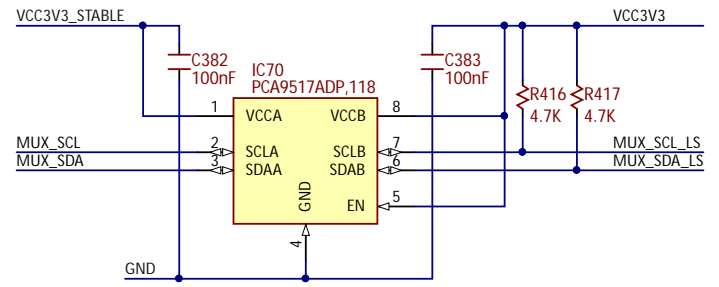
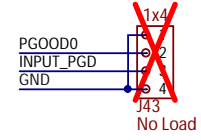
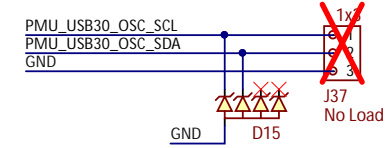
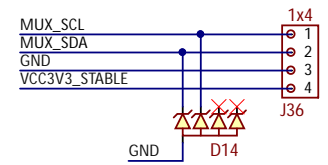
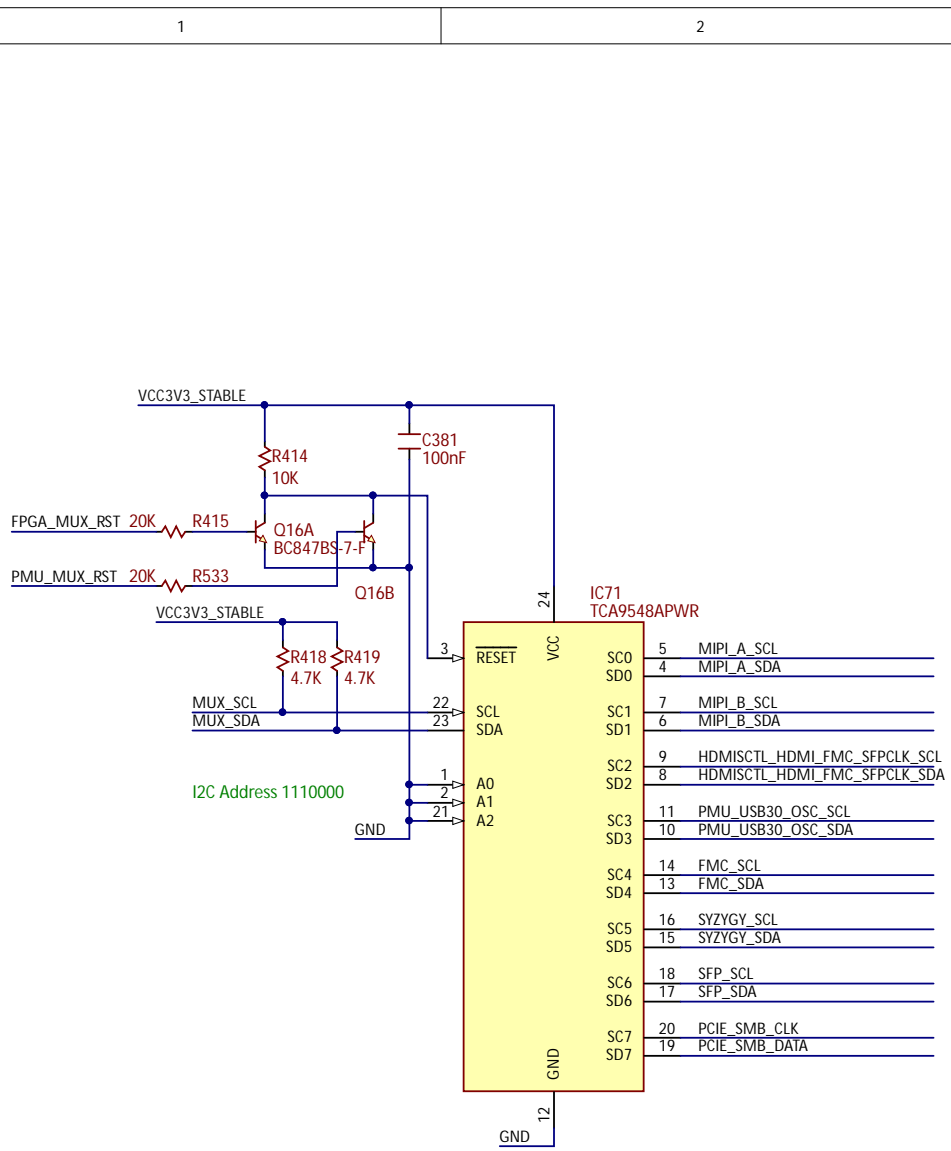


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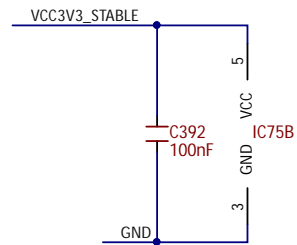
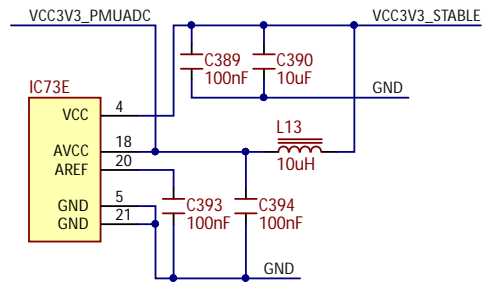
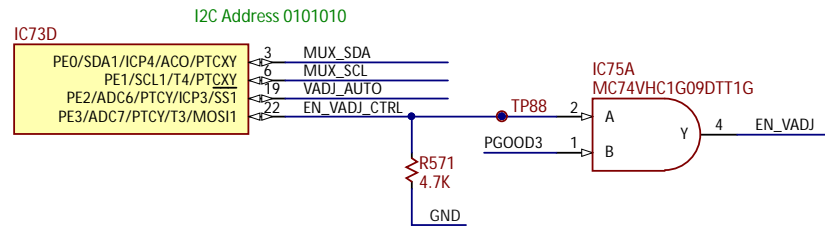
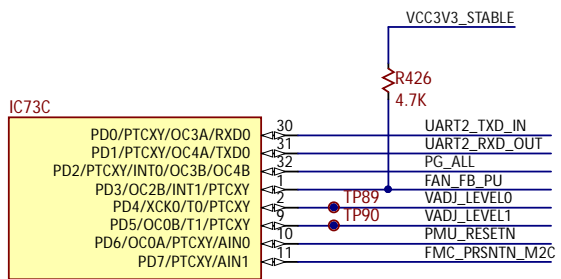
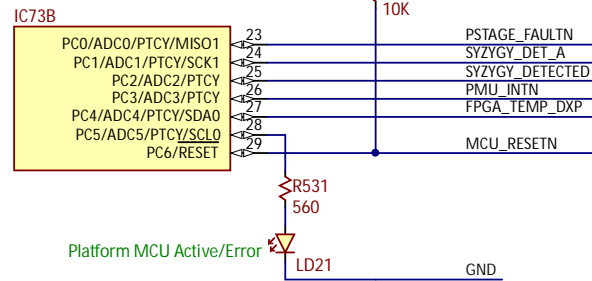
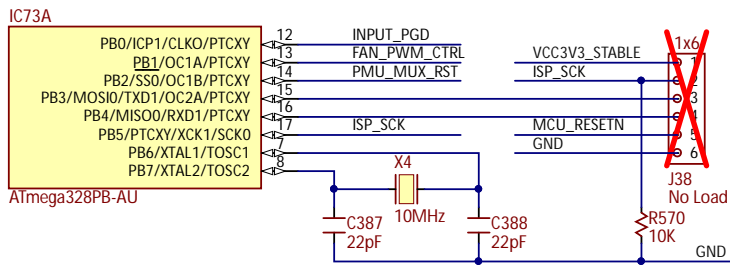
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Circuit DDR4 SODIMM SUPPLIES		 A National Instruments Company
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Circuit	I2C Interfaces		
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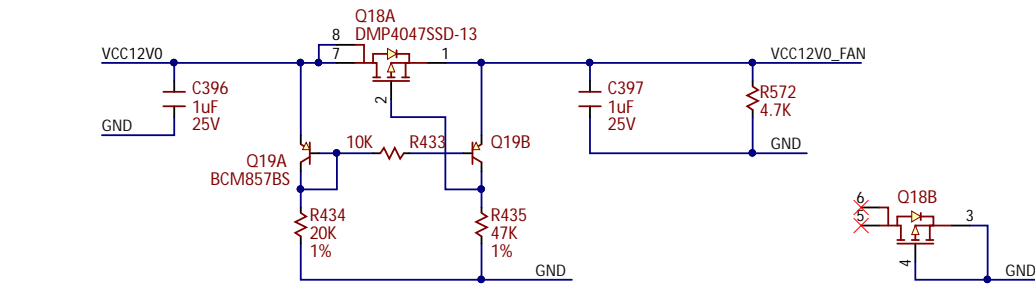
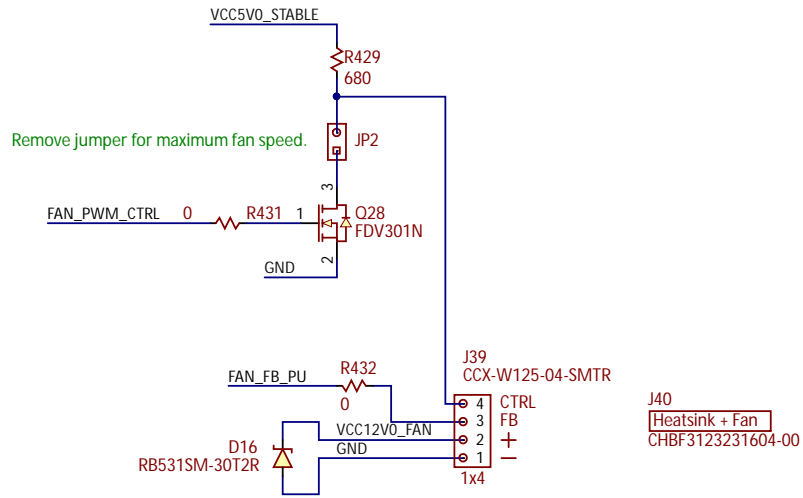
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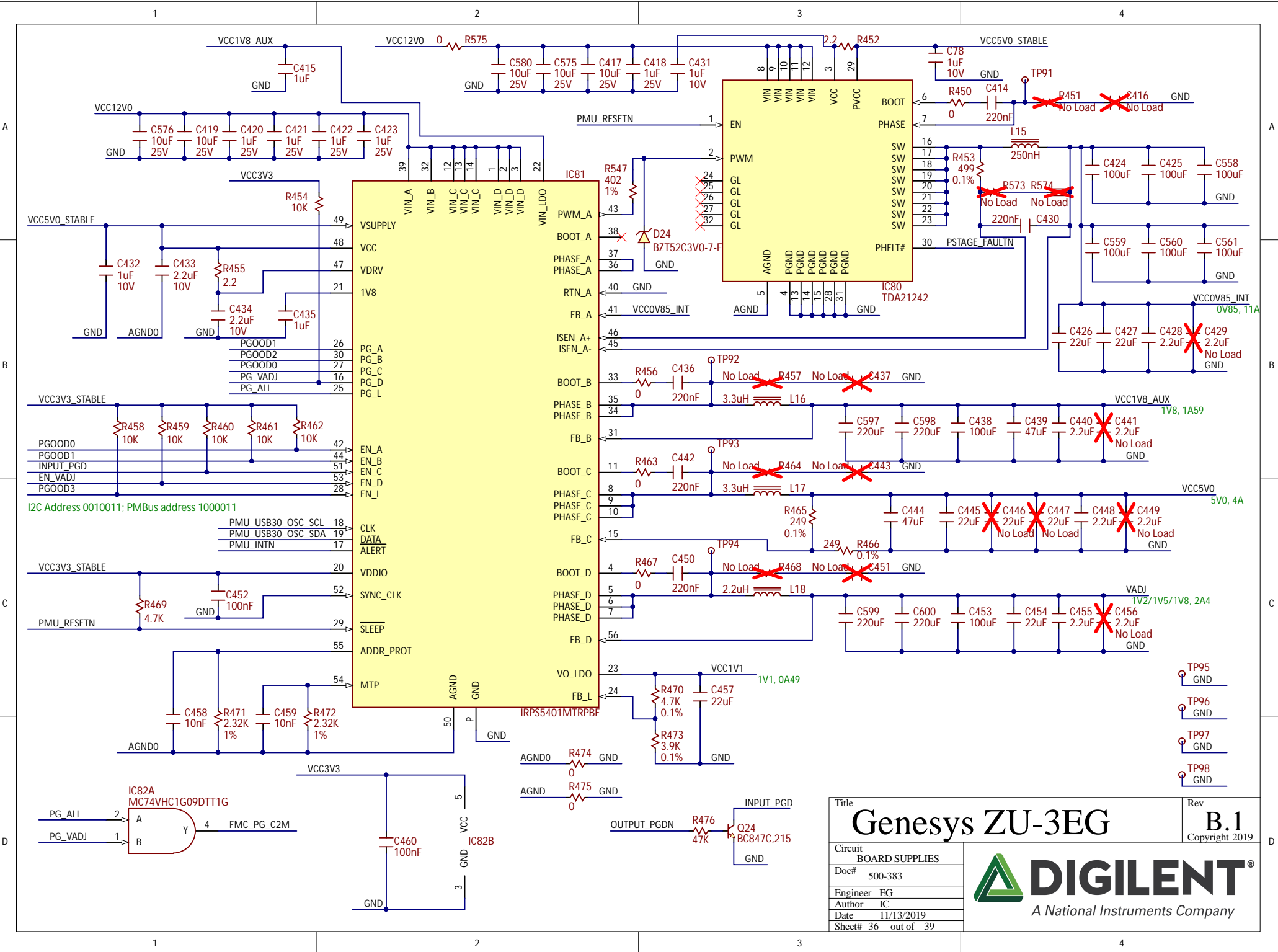
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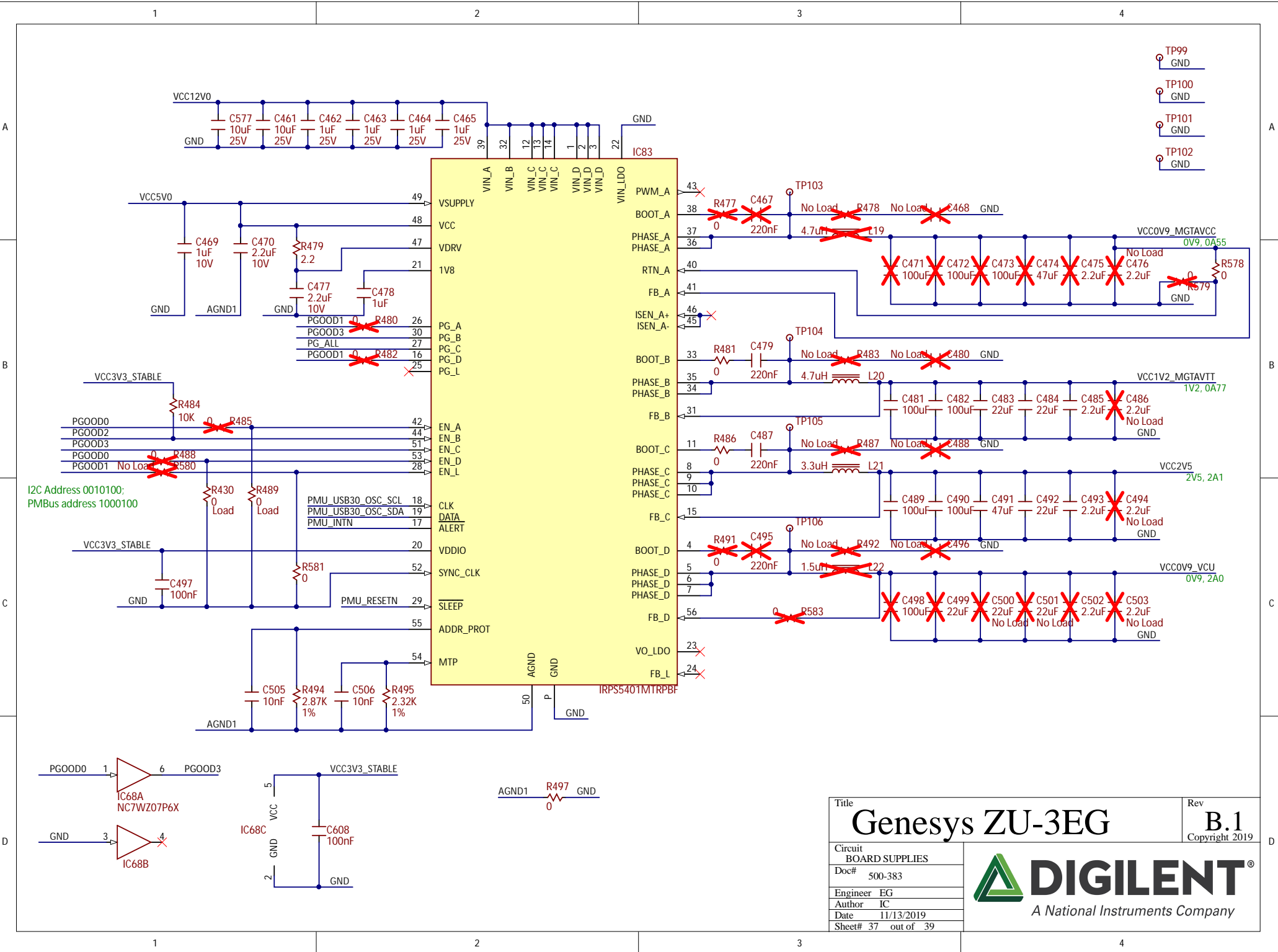
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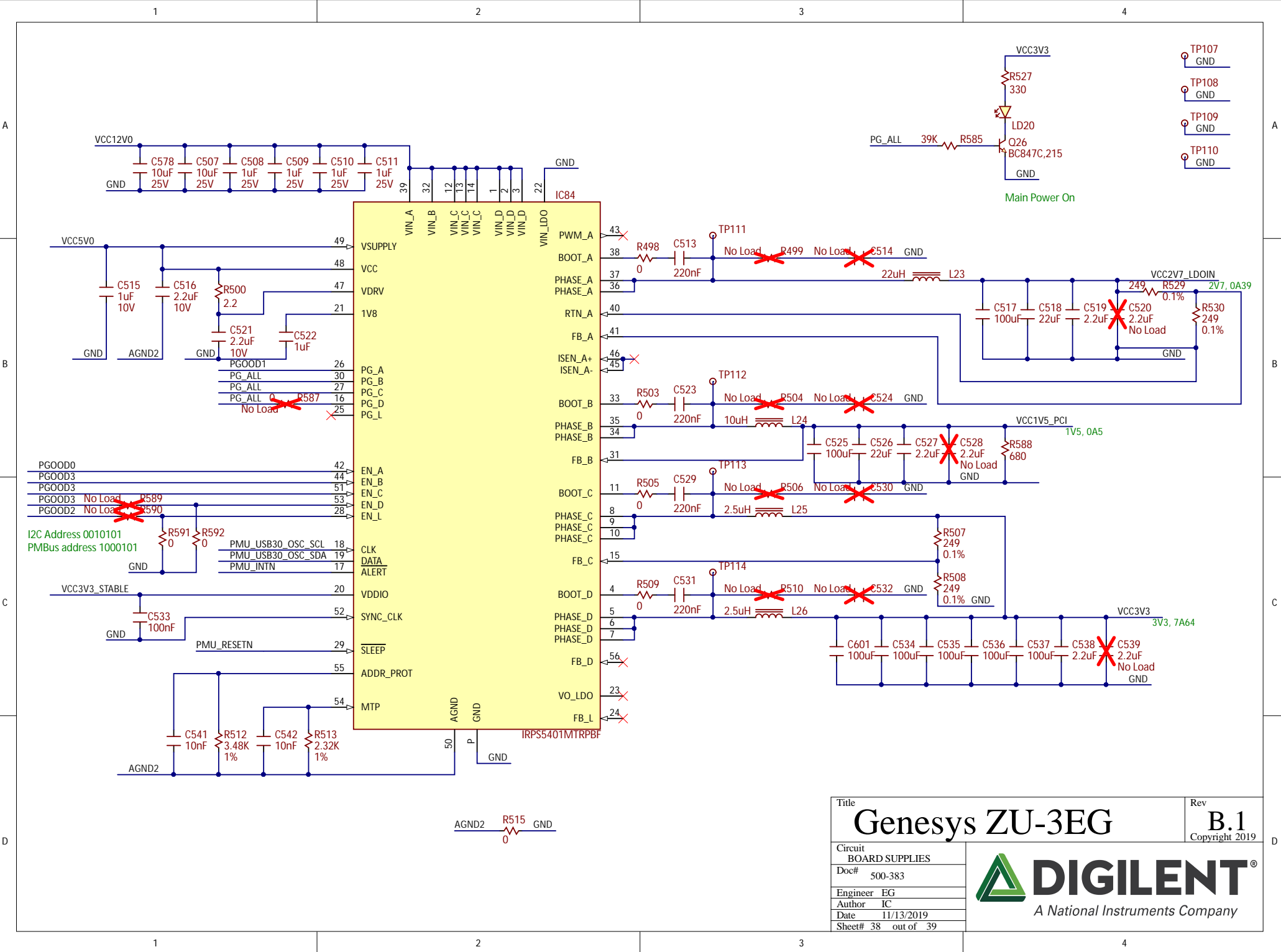


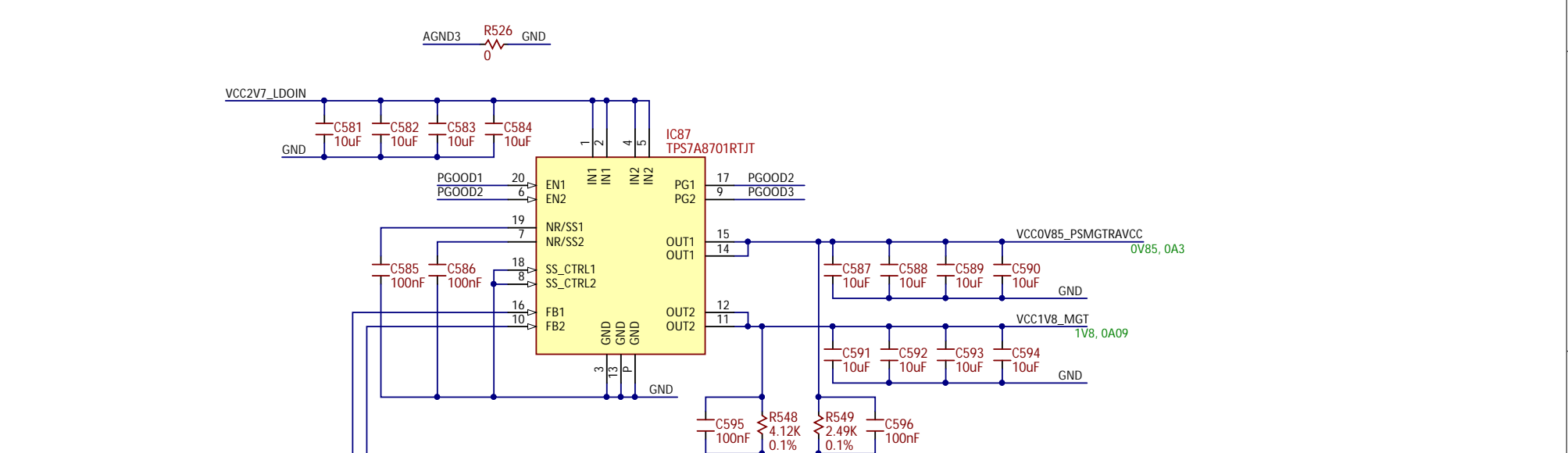
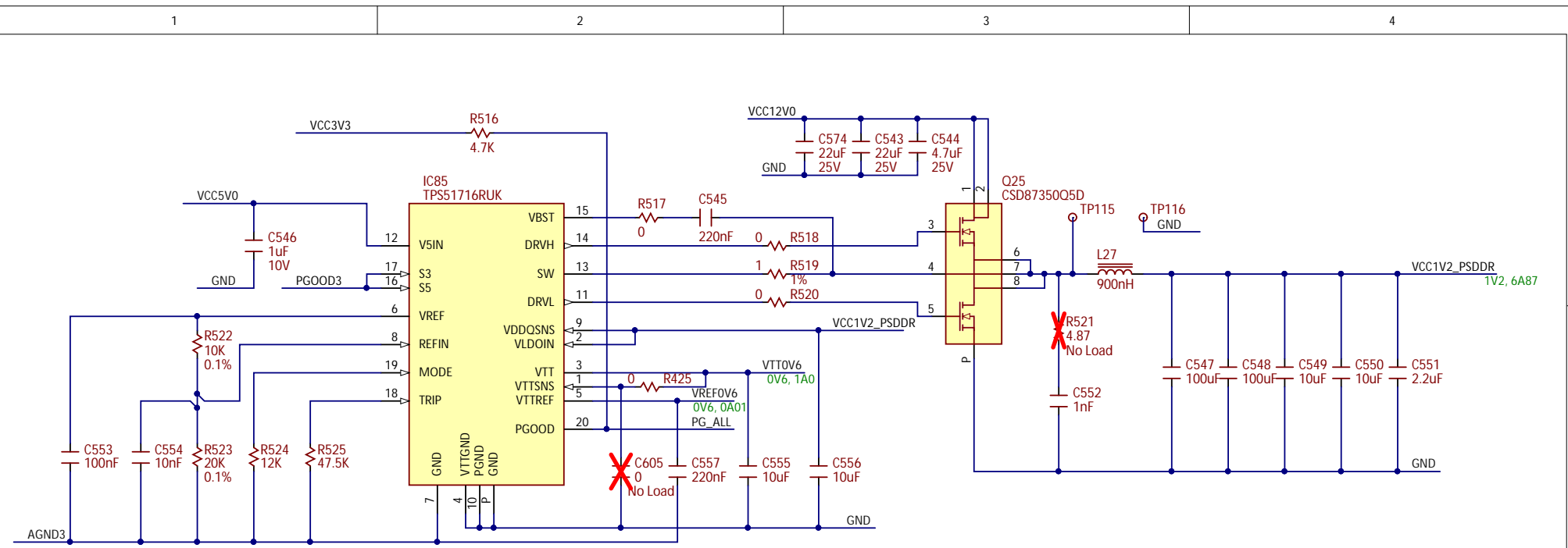
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