

[illegible]

POWER

I2C

XCLK

MIPI Output

The diagram illustrates the MIPI Output interface for the F32Q-1A7H1-11022 module. It shows a 22-pin connector (J1) with the following pin assignments:

- 1: Ground
- 2: CAM_D0_N
- 3: CAM_D0_P
- 4: Ground
- 5: CAM_D1_N
- 6: CAM_D1_P
- 7: Ground
- 8: CAM_C_N
- 9: CAM_C_P
- 10: Ground
- 11: CAM_D2_N
- 12: CAM_D2_P
- 13: Ground
- 14: CAM_D3_N
- 15: CAM_D3_P
- 16: Ground
- 17: POWER_EN
- 18: LED_EN
- 19: Ground
- 20: SIOC
- 21: SIOD
- 22: Ground

The module is powered by a +3V3 supply connected to pin 18 (POWER_EN) and a 10uF capacitor connected to pin 22 (SIOC). The module is labeled F32Q-1A7H1-11022.

Test Point

TP1 — XVS Protect — TP2 — XHS Protect — TP3 — GND

M12 Lens Mount

The diagram shows a circular lens mount. A blue circle represents the lens, with a smaller blue circle inside it labeled "GND". A red line with an arrow points from the "GND" circle to a red "X" mark. Below the lens, the text "FixedHole" is written in blue. Above the lens, the text "H1" is written in blue.

XCLK

The diagram illustrates the XCLK circuit. A 24MHz oscillator (G1) provides the clock signal. The circuit includes a 10uF capacitor (C1) and a 10k resistor (R6) connected to the clock signal line. The clock signal is labeled XCLK. The LED_EN signal is also shown, connected to the XCLK line through a 10k resistor (R7).